

Description

ATSENSE-101/ATSENSE-301(H) are multi-channel analog front end devices which integrate three or seven simultaneously sampled Sigma-Delta A/D converters, a high-precision voltage reference with up to 10 ppm/°C temperature stability (H-versions), a programmable current signal amplification, a temperature sensor and an SPI interface. When used in data acquisition and energy measurement applications in combination with the Atmel® ATSAM4C device family that features a dedicated Cortex®-M4 processor and metrology library and a variety of sensors including Shunt, CT and Rogowski coils, the ATSENSE-101/ATSENSE-301(H) exceeds ANSI C12.20-2002 and IEC 62053-22 metering accuracy classes of up to 0.2% over 3000:1 current range.

Features

- Analog Front End
 - Single-phase (ATSENSE-101) or Polyphase (ATSENSE-301(H)) Energy Metering Analog Front End Suitable for Atmel MCUs and Metrology Library
 - Compliant with Class 0.2 Standards (ANSI C12.20-2002 and IEC 62053-22)
 - Three or Seven Sigma-Delta ADC Measurement Channels: One or Three Voltages, Two or Four Currents, 102 dB Dynamic Range
 - Current Channels with Pre-Gain (x1, x2, x4, x8)
 - Supports Shunt, Current Transformer and Rogowski Coils
 - Dedicated Current Channel for Anti-tamper Measurement
 - Integrated SINC Decimation Filters. Output Data Rate: 16 kSps typical
 - Integrated 2.8V LDO Regulator to Supply Analog Functions
 - 3.0V to 3.6V Operation, Ultra Low Power: < 2.5 mW typical/Channel @ 3.3V
 - Specified for $T_J = [-40^{\circ}\text{C}; +100^{\circ}\text{C}]$
- Precision Voltage Reference
 - Standard 1.2V Output Voltage with Possible External Bypass
 - Temperature Drift: 50 ppm typical (ATSENSE-101/ATSENSE-301)
 - Temperature Drift: 10 ppm typical (ATSENSE-301H)
 - Factory-measured Temperature Drift and Die Temperature Sensor to Perform Software Correction
- Digital Interface

- 8 MHz Serial Peripheral Interface (SPI) Compatible Mode 1 (8-bit) for ADC Data and AFE Controls
- Interrupt Output Line Signaling ADC End-of-Conversion, Underrun and Overrun
- Package
 - 32-lead TQFP, 7 x 7 x 1.4 mm
 - 20-lead SOIC, 12.8 x 7.5 x 2.3 mm

1. Block Diagrams

Figure 1-1. ATSENSE-301(H) Functional Block Diagram

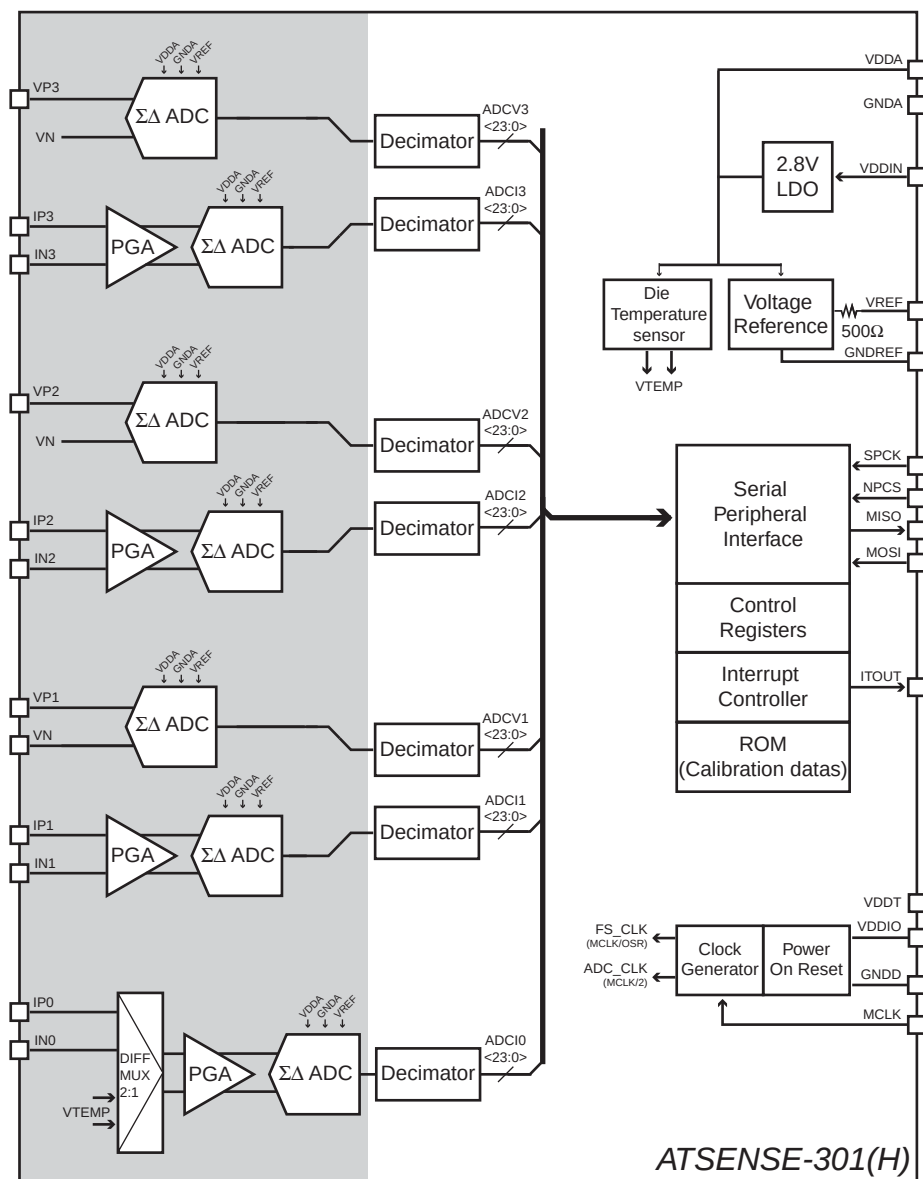
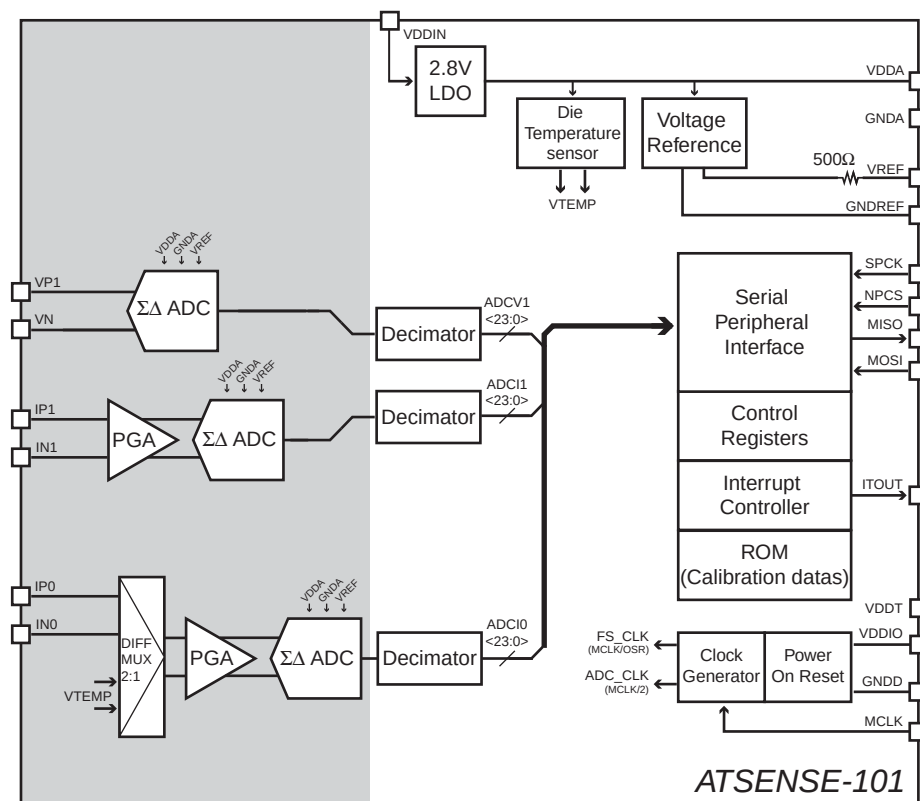


Figure 1-2. ATSENSE-101 Functional Block Diagram



2. Package and Pinout

2.1 ATSENSE-301(H)

Figure 2-1. 32-lead LQFP Package

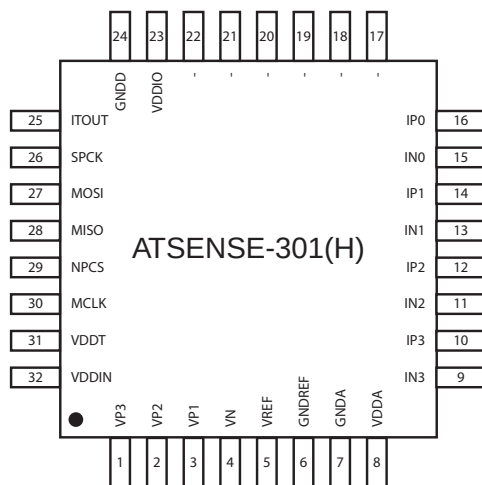


Table 2-1. ATSENSE-301(H) Pin Description

Pin Name	I/O	Pin Number	Type	Function
VP3	Input	1	Analog	Voltage channel 3, positive input
VP2	Input	2	Analog	Voltage channel 2, positive input
VP1	Input	3	Analog	Voltage channel 1, positive input
VN	Input	4	Analog	Voltage channels negative input
VREF	In / Out	5	Analog	Voltage reference output and ADCs reference buffer input
GNDREF	Ground	6	Ground	Voltage reference ground pin
GNDA	Ground	7	Ground	Ground pin for low noise analog circuits and low noise negative ADC reference
VDDA	In / Out	8	Analog	2.8V LDO output and analog circuits power supply input
IN3	Input	9	Analog	Current channel 3, negative input
IP3	Input	10	Analog	Current channel 3, positive input
IN2	Input	11	Analog	Current channel 2, negative input
IP2	Input	12	Analog	Current channel 2, positive input
IN1	Input	13	Analog	Current channel 1, negative input
IP1	Input	14	Analog	Current channel 1, positive input
IN0	Input	15	Analog	Current channel 0 (Tamper), negative input
IP0	Input	16	Analog	Current channel 0 (Tamper), positive input
-	-	17 .. 22	-	Not connected. Connect to ground
VDDIO	Input	23	Power	Power supply input pin for digital I/O and digital core circuits
GNDD	Ground	24	Ground	Ground pin for digital I/O and digital core circuits

Table 2-1. ATSENSE-301(H) Pin Description

Pin Name	I/O	Pin Number	Type	Function
ITOUT	Output	25	Digital	Interrupt output line. Open-drain
SPCK	Input	26	Digital	SPI port: serial clock
MOSI	Input	27	Digital	SPI port: master output slave input
MISO	Output	28	Digital	SPI port: master input slave output
NPCS	Input	29	Digital	SPI port: active-low chip select
MCLK	Input	30	Digital	Master Clock Input
VDDT	Input	31	Power	Pin reserved for test. Connect to VDDIN / VDDIO plane
VDDIN	Input	32	Power	2.8V LDO power supply input pin

2.2 ATSENSE-101

Figure 2-2. 20-lead SOIC Package

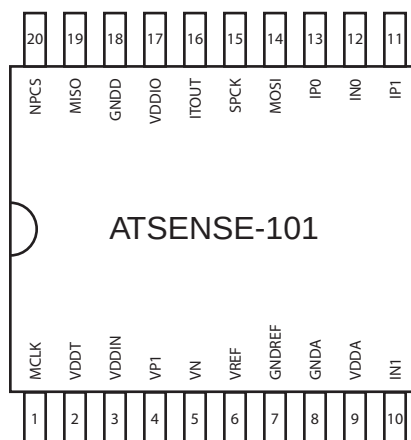
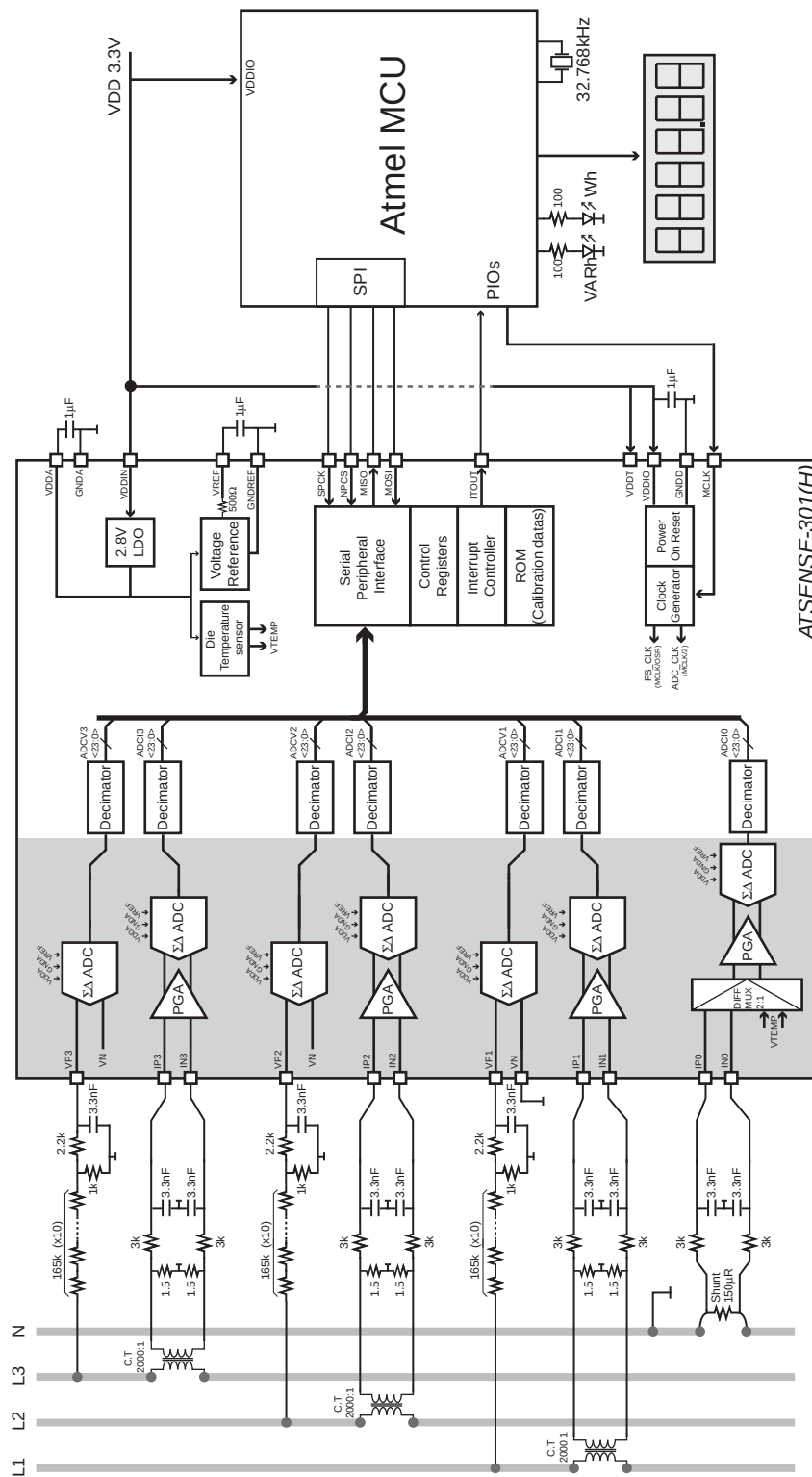


Table 2-2. ATSENSE-101 Pin Description

Pin Name	I/O	Pin Number	Type	Function
MCLK	Input	1	Digital	Master Clock Input
VDDT	Input	2	Power	Pin reserved for test. Connect to VDDIN / VDDIO plane
VDDIN	Input	3	Power	2.8V LDO Power supply input pin
VP1	Input	4	Analog	Voltage Channel 1, positive input
VN	Input	5	Analog	Voltage Channel negative input
VREF	In / Out	6	Analog	Voltage reference output and ADCs reference buffer input
GNDREF	Ground	7	Ground	Voltage reference ground pin
GNDA	Ground	8	Ground	Ground pin for low noise analog circuits and low noise negative ADC reference
VDDA	In / Out	9	Analog	2.8V LDO output and analog circuits power supply input
IN1	Input	10	Analog	Current Channel 1, negative input
IP1	Input	11	Analog	Current Channel 1, positive input
IN0	Input	12	Analog	Current Channel 0 (Tamper), negative input
IP0	Input	13	Analog	Current Channel 0 (Tamper), positive input
MOSI	Input	14	Digital	SPI port: Master Output Slave Input
SPCK	Input	15	Digital	SPI port: Serial clock
ITOUT	Output	16	Digital	Interrupt output line. Open Drain
VDDIO	Input	17	Power	Power supply input pin for digital I/O and digital core circuits
GNDD	Ground	18	Ground	Ground pin for digital I/O and digital core circuits
MISO	Output	19	Digital	SPI port: master input slave output
NPCS	Input	20	Digital	SPI port: active-low chip select

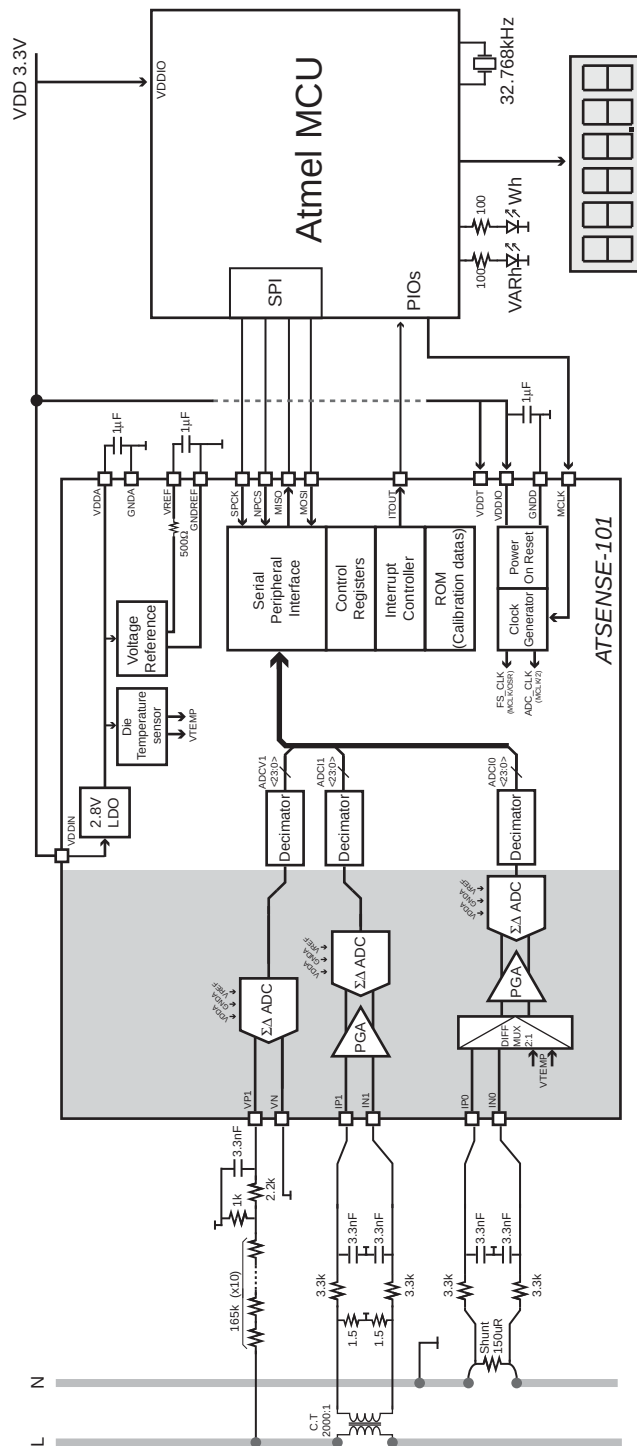
3. Application Block Diagram

Figure 3-1. ATSENSE-301(H) Typical Application Block Diagram



Typical 200A (Imax), 3-phase, 4-Wire Smart meter
based on Atmel Metrology Solution

Figure 3-2. ATSENSE-101 Typical Application Block Diagram



Typical 100A (Imax), Single-phase with anti-tamper Smart meter based on Atmel Metrology Solution

4. Functional Description

4.1 Conversion Channels

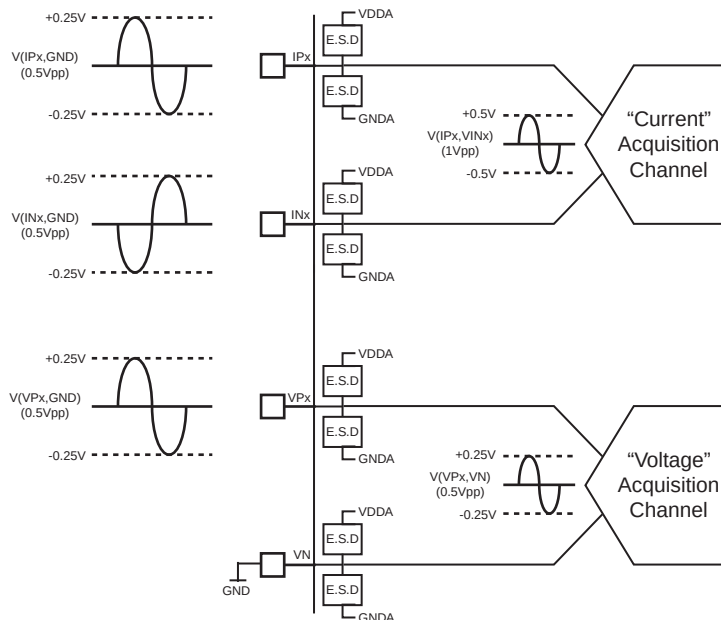
ATSENSE-101/ATSENSE-301(H) have three types of acquisition channels:

- Voltage channels
- Current channels
- Tamper and temperature channel

All these channels are built around the same Sigma-Delta A/D converter. The voltage reference of this converter is the VREF pin voltage referred to ground (GNDA pin). This reference voltage can be internally or externally sourced. The converter's sampling rate is MCLK/4, typically 1.024 MHz. An external low-pass filter, typically a passive R-C network, is required at each ADC input to reject frequency images around this sampling frequency (anti-alias).

ATSENSE-101/ATSENSE-301(H) analog inputs are designed to sample 0V centered signals. As these inputs have internal ESD protection devices connected to GNDA, the maximum input signal level defined in the electrical characteristics must be respected to avoid leakages in these devices. This is typically $\pm 0.25\text{V}$. Refer to [Figure 4-1](#), "Analog Inputs: Recommended Input Range".

Figure 4-1. Analog Inputs: Recommended Input Range



Voltage channels have single-ended inputs referred to the VN pin. This pin must be connected to a low noise ground. The user must take care that no I.R drop on the ground net is sampled by the ADC by non-optimum connection of the VN pin.

Current channels have a programmable gain amplifier (PGA) to accommodate low input signals. The PGA improves the dynamic range of the channel as the input referred noise gets lower when gain gets higher. The PGA does not introduce any delay or bandwidth limitation on the current channels compared to the voltage channels. The channels (voltage or current) are always sampled synchronously. The input impedance of the PGA depends on the programmed gain.

The tamper channel features an input multiplexer to perform both the neutral current measurement and the die temperature measurement. The tamper channel has a PGA to accommodate low output-level current sensors. Programmed gain can be changed when switching from the tamper to the die temperature sensor source.

4.2 Voltage Reference, Die Temperature Measurement and Calibration Registers

4.2.1 Voltage Reference

ATSENSE-101/ATSENSE-301(H) embed an analog voltage reference with a typical output voltage of 1.144V. The temperature drift of the voltage reference can be approximated by a linear fit. For H grade parts, this temperature drift is measured during manufacturing and stored in the calibration registers (ROM). More particularly, the parts are measured twice: at a low temperature, TL, and at a high temperature, TH. At both temperatures TL and TH, VREF voltage and ADC_TEMP_OUT (ADC I/O reading of the temperature sensor) parameters are saved. From the stored data, the user can implement a software compensation of the voltage reference.

4.2.2 Die Temperature Sensor

To measure the internal die temperature, ATSENSE-101/ATSENSE-301(H) embed a dedicated analog die temperature sensor that is multiplexed on the tamper channel (ADC I/O). By measuring the die temperature periodically and by using the calibration bits, the channel gain drifts over temperature due to the voltage reference can be corrected.

To set the ADC to measure the temperature sensor, the user must set the TEMPMEAS bit in ADC I/O control register and ensure that the channel gain is set to x1 (0dB).

Once the temperature measurement is selected, the ADC starts to output samples corresponding to the temperature sensor. The first four samples account for internal digital filters settling and must be ignored. Then, in order to have a repeatable temperature acquisition, the user must average the ADC output over a minimum of 64 samples. Done this way, the temperature acquisition measurement exhibits a standard deviation of less than 0.25°C in repeatability.

To calculate the real die temperature from the ADC acquisition, the following formula applies:

$$T_J(^{\circ}\text{C}) = (\text{ADC_TEMP_OUT} / 2^{24} \times 1.144 - 0.110) / 0.00049$$

where ADC_TEMP_OUT is the 24-bit output of ADC I/O, averaged over 64 samples. Example: If ADC_TEMP_OUT = 1777345, the corresponding die temperature is $T_J = 22.8^{\circ}\text{C}$.

Because the temperature sensor is not offset-calibrated, the absolute temperature reading exhibits a large deviation (typically $\pm 15^{\circ}\text{C}$).

4.2.3 Calibration Registers

The registers involved in the voltage reference compensation are listed in [Table 4-1](#). The four parameters stored, VREF and ADC_TEMP_OUT at TL and TH, are:

- REF_TL[11:0] and REF_TH[11:0]
- TEMP_TL[11:0] and TEMP_TH[11:0]

The following rule applies to recover the real values of VREF from the 12-bit coded values in the product registers:

$$\text{VREF(TL)} = 1.120\text{V} + \text{REF_TL}[11:0] \times 25\mu\text{V}$$

$$\text{VREF(TH)} = 1.120\text{V} + \text{REF_TH}[11:0] \times 25\mu\text{V}$$

Note: REF_TL[11:0] and REF_TH[11:0] are unsigned 12-bit integers.

The following rule applies to recover the real values of ADC_TEMP_OUT from the 12-bit coded values in the product registers:

$$\text{ADC_TEMP_OUT}[23:0](\text{TL}) = \text{TEMP_TL}[11:0] \ll 12$$

$$\text{ADC_TEMP_OUT}[23:0](\text{TH}) = \text{TEMP_TH}[11:0] \ll 12$$

Note: TEMP_TL[11:0] and TEMP_TH[11:0] are signed 12-bit integers.

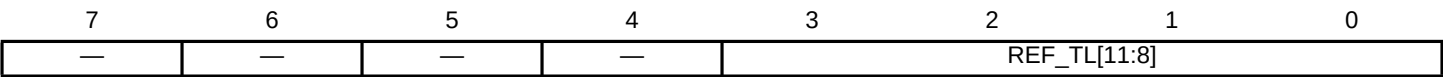
Table 4-1. Calibration Register Mapping

Offset	Register	Name	Access	Reset
0x41	Voltage Reference Value at TL: MSB	REF_TL_11_8	Read	0x-0
0x42	Voltage Reference Value at TL: LSB	REF_TL_7_0	Read	0x00
0x43	Temperature Sensor Value (read by ADC) at TL: MSB	TEMP_TL_11_8	Read	0x-0
0x44	Temperature Sensor Value (read by ADC) at TL: LSB	TEMP_TL_7_0	Read	0x00
0x45	Voltage Reference Value at TH: MSB	REF_TH_11_8	Read	0x-0
0x46	Voltage Reference Value at TH: LSB	REF_TH_7_0	Read	0x00
0x47	Temperature Sensor Value (read by ADC) at TH: MSB	TEMP_TH_11_8	Read	0x-0
0x48	Temperature Sensor Value (read by ADC) at TH: LSB	TEMP_TH_7_0	Read	0x00

4.3 Voltage Reference Value at TL: MSB

Name: REF_TL_11_8

Access: Read-only

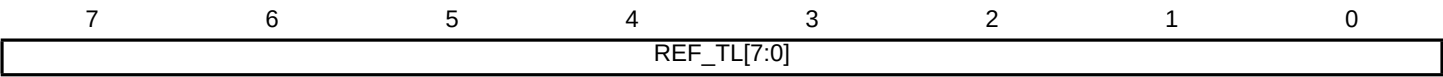


- REF_TL[11:8]: 4 MSB of REF_TL[11:0]

4.4 Voltage Reference Value at TL: LSB

Name: REF_TL_7_0

Access: Read-only



- REF_TL[7:0]: 8 LSB of REF_TL[11:0]

4.5 Temperature Sensor Value at TL: MSB

Name: TEMP_TL_11_8

Access: Read-only

7	6	5	4	3	2	1	0
—	—	—	—	TEMP_TL[11:8]			

- TEMP_TL[11:8]: 4 MSB of TEMP_TL[11:0]

4.6 Temperature Sensor Value at TL: LSB

Name: TEMP_TL_7_0

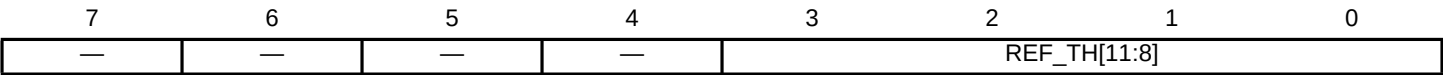
Access: Read-only

7	6	5	4	3	2	1	0
TEMP_TL[7:0]							

- TEMP_TL[7:0]: 8 LSB of TEMP_TL[11:0]

4.7 Voltage Reference Value at TH: MSB

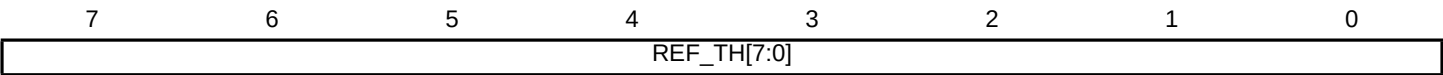
Name: REF_TH_11_8
Access: Read-only



- REF_TH[11:8]: 4 MSB of REF_TH[11:0]

4.8 Voltage Reference Value at TH: LSB

Name: REF_TH_7_0
Access: Read-only

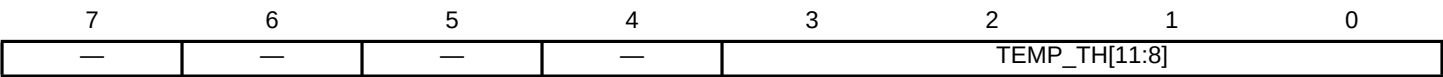


- REF_TH[7:0]: 8 LSB of REF_TH[11:0]

4.9 Temperature Sensor Value at TH: MSB

Name: TEMP_TH_11_8

Access: Read-only

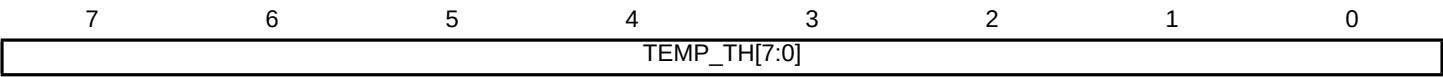


- TEMP_TH[11:8]: 4 MSB of TEMP_TH[11:0]

4.10 Temperature Sensor Value at TH: LSB

Name: TEMP_TH_7_0

Access: Read-only



- TEMP_TH[7:0]: 8 LSB of TEMP_TH[11:0]

4.11 Correction Algorithm

For H-grade products, it is possible to compensate the drift of the voltage reference by using the calibration registers described above. The following formula applies to estimate VREF at a given temperature:

$$VREF(ADC_TEMP_OUT) = VREF(TL) + \frac{(ADC_TEMP_OUT - TEMP_TL)}{(TEMP_TH - TEMP_TL)} \cdot (VREF(TH) - VREF(TL))$$

where:

- VREF(ADC_TEMP_OUT): Estimated VREF value when the temperature sensor reading is ADC_TEMP_OUT
- VREF(TL): VREF value at temperature TL retrieved from REF_TL[11:0]
- VREF(TH): VREF value at temperature TH retrieved from REF_TH[11:0]
- TEMP(TL): ADC_TEMP_OUT value at temperature TL retrieved from TEMP_TL[11:0]
- TEMP(TH): ADC_TEMP_OUT value at temperature TH retrieved from TEMP_TH[11:0]

5. SPI Controller

5.1 Description

The SPI controller is an interface between

- the serial peripheral interface communication port
- the decimation filter output data in 2's complement format
- the analog functions (ADC, LDO and reference voltage)

The SPI port provides read/write access to internal registers ([Table 4-1 on page 11](#)). This serial port features a burst transmission mode with variable data size that captures up to 7 x 32-bit ADC output results into one single access.

5.2 SPI Serial Port

5.2.1 Description

The SPI interface protocol permits writing to and/or reading registers. Moreover, a burst mode allows the fast acquisition of multiple registers or a write on multiple registers. With this function, the size of the data can easily vary. For example, two adjacent registers can be accessed at the same time by addressing the first register (lowest address value) and extending the quantity of serial clock edges.

The SPI interface is compatible with SPI modes 1 and 2. Data are latched on falling edges of SCLK while they are generated on the rising edges of SCLK. The idle state of SCLK can be either high or low.

5.2.2 Protocol

A transfer occurs when the SCSB signal is low. The incoming stream on MOSI is decoded on SCLK falling edge.

The first received bit indicates the direction of the operation, where 0 indicates a write and 1 a read.

The seven subsequent bits contain the address of the register to read or write.

The following bytes are data which are either emitted on the MISO line in case of a read operation, or decoded on the MOSI line in case of a write operation.

The first data address corresponds to the first decoded address. The address pointer is then incremented each time a new byte is read or written.

The operation ends when SCSB goes high.

If SCSB goes high before the end of a byte transfer, the current byte operation is cancelled. For a read operation, no more data are sent on the MISO line. For a write operation, nothing is written into the currently decoded address. All previous byte operations are valid.

Figure 5-1. MODE 1 Multi-Byte Write Operation

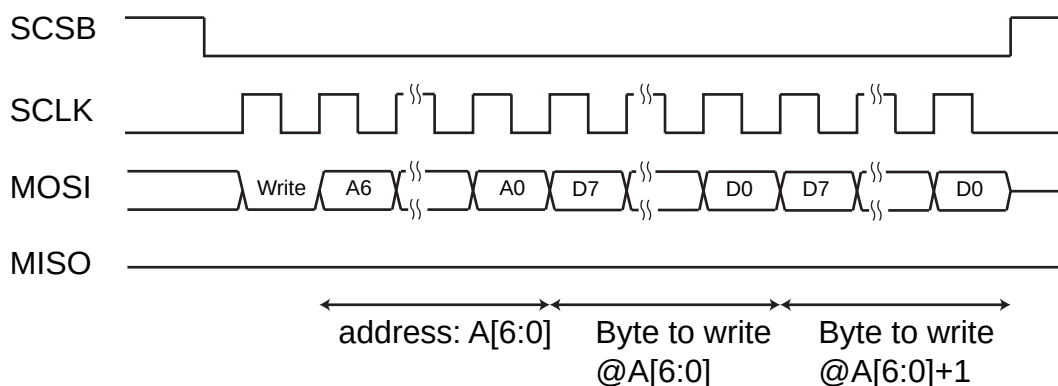


Figure 5-2. MODE 2 Multi-Byte Write Operation

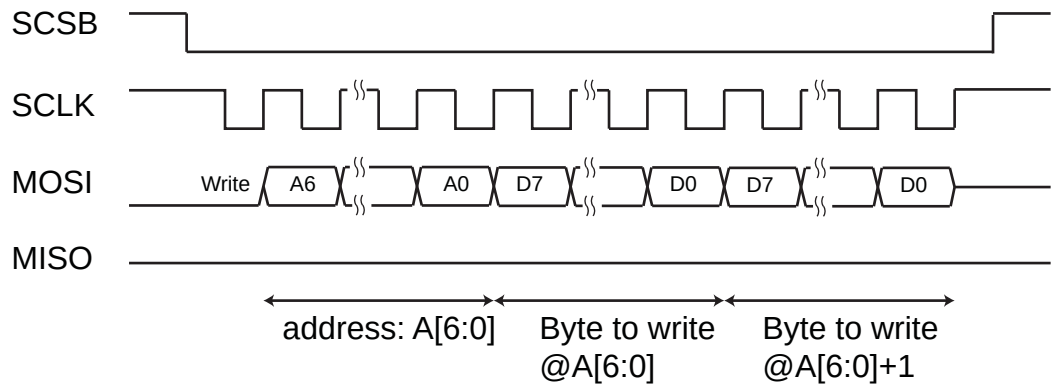


Figure 5-3. MODE 1 Multi-Byte Read Operation

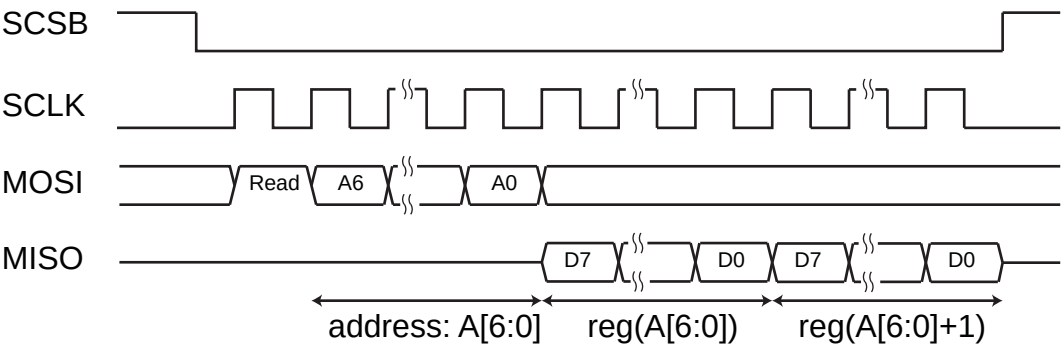
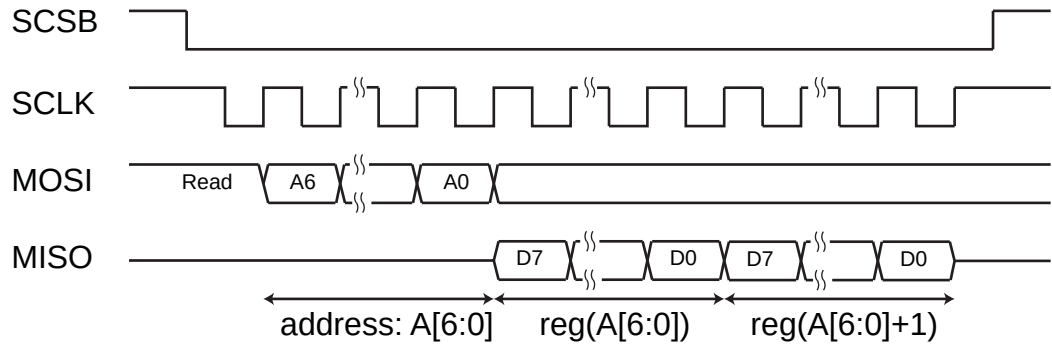


Figure 5-4. MODE 2 Multi-Byte Read Operation



6. Interrupt Controller

The Interrupt Controller generates three interrupts:

- ADC ready interrupt
- Overrun interrupt
- Underrun interrupt

The interrupts can be detected by either polling the Interrupt Status register (ITSR) and/or by configuring the ITOUT output line. Because it is open-drain, this output needs to be pulled-up to VDDIO.

When activated, the ITOUT line goes low when an interrupt event occurs. It goes into Hi-Z state as soon as the interrupt source has been reset.

Please refer to [“Output Interrupt Line Control Register” on page 40](#), [“Interrupt Control Register” on page 41](#) and [“Interrupt Status Register” on page 42](#) for more information on the interrupt line configuration

6.1 ADC Ready

The ADC_RDY interrupt rises at each new conversion frame, thus when an ADC is enabled, it reports that a new set of data is available.

It is reset either on the read of at least one ADC register (addresses from ADCI0_TAG to ADCV3_7_0) or on the read of the status register.

As the user may not need all converted values of the ADCs, only the first access to an ADC data is taken into account to reset this interrupt.

6.2 Overrun

If ADC data acquisition registers are accessed twice within the same conversion period, the OVRES interrupt rises.

It is reset on the read of the status register.

6.3 Underrun

If two synchronous signals occur without any ADC data acquisition, the UNDES interrupt rises.

It is reset on the read of the status register.

7. SPI Controller User Interface

Table 7-1. Register Mapping

Offset	Register	Name	Access	Reset
0x00 ⁽²⁾	ADCI0_TAG	ADCI0_TAG	Read-only	0x01
0x01 (0x00 ⁽¹⁾)	ADCI0_23_16	ADCI0_23_16	Read-only	0x00
0x02 (0x01 ⁽¹⁾)	ADCI0_15_8	ADCI0_15_8	Read-only	0x00
0x03 ⁽²⁾	ADCI0_7_0	ADCI0_7_0	Read-only	0x00
0x04 ⁽²⁾	ADCI1_TAG	ADCI1_TAG	Read-only	0x02
0x05 (0x02 ⁽¹⁾)	ADCI1_23_16	ADCI1_23_16	Read-only	0x00
0x06 (0x03 ⁽¹⁾)	ADCI1_15_8	ADCI1_15_8	Read-only	0x00
0x07 ⁽²⁾	ADCI1_7_0	ADCI1_7_0	Read-only	0x00
0x08 ⁽²⁾	ADCV1_TAG	ADCV1_TAG	Read-only	0x03
0x09 (0x04 ⁽¹⁾)	ADCV1_23_16	ADCV1_23_16	Read-only	0x00
0x0a (0x05 ⁽¹⁾)	ADCV1_15_8	ADCV1_15_8	Read-only	0x00
0x0b ⁽²⁾	ADCV1_7_0	ADCV1_7_0	Read-only	0x00
0x0c ⁽²⁾	ADCI2_TAG ⁽³⁾	ADCI2_TAG	Read-only	0x04
0x0d (0x06 ⁽¹⁾)	ADCI2_23_16 ⁽³⁾	ADCI2_23_16	Read-only	0x00
0x0e (0x07 ⁽¹⁾)	ADCI2_15_8 ⁽³⁾	ADCI2_15_8	Read-only	0x00
0x0f ⁽²⁾	ADCI2_7_0 ⁽³⁾	ADCI2_7_0	Read-only	0x00
0x10 ⁽²⁾	ADCV2_TAG ⁽³⁾	ADCV2_TAG	Read-only	0x05
0x11 (0x08 ⁽¹⁾)	ADCV2_23_16 ⁽³⁾	ADCV2_23_16	Read-only	0x00
0x12 (0x09 ⁽¹⁾)	ADCV2_15_8 ⁽³⁾	ADCV2_15_8	Read-only	0x00
0x13 ⁽²⁾	ADCV2_7_0 ⁽³⁾	ADCV2_7_0	Read-only	0x00
0x14 ⁽²⁾	ADCI3_TAG ⁽³⁾	ADCI3_TAG	Read-only	0x06
0x15 (0x0a ⁽¹⁾)	ADCI3_23_16 ⁽³⁾	ADCI3_23_16	Read-only	0x00
0x16 (0x0b ⁽¹⁾)	ADCI3_15_8 ⁽³⁾	ADCI3_15_8	Read-only	0x00
0x17 ⁽²⁾	ADCI3_7_0 ⁽³⁾	ADCI3_7_0	Read-only	0x00
0x18 ⁽²⁾	ADCV3_TAG ⁽³⁾	ADCV3_TAG	Read-only	0x07
0x19 (0x0c ⁽¹⁾)	ADCV3_23_16 ⁽³⁾	ADCV3_23_16	Read-only	0x00
0x1a (0x0d ⁽¹⁾)	ADCV3_15_8 ⁽³⁾	ADCV3_15_8	Read-only	0x00
0x1b ⁽²⁾	ADCV3_7_0 ⁽³⁾	ADCV3_7_0	Read-only	0x00
0x20	ADCI0 Controls	SDI0	Read/Write	0x00
0x21	ADCI1 Controls	SDI1	Read/Write	0x00
0x22	ADCV1 Controls	SDV1	Read/Write	0x00
0x23	ADCI2 Controls ⁽³⁾	SDI2	Read/Write	0x00
0x24	ADCV2 Controls ⁽³⁾	SDV2	Read/Write	0x00
0x25	ADCI3 Controls ⁽³⁾	SDI3	Read/Write	0x00
0x26	ADCV3 Controls ⁽³⁾	SDV3	Read/Write	0x00

Table 7-1. Register Mapping

Offset	Register	Name	Access	Reset
0x27	Analog Controls	ANA_CTRL	Read/Write	0x00
0x28	ATSENSE Configuration	ATCFG	Read/Write	0x03
0x29	ATSENSE Status	ATSR	Read-only	—
0x2a	Output Interrupt Line Control	ITOUTCR	Read/Write	0x04
0x2b	Interrupt Control	ITCR	Read/Write	0x00
0x2c	Interrupt Status	ITSR	Read-only	0x00
0x2d	Software Reset	SOFT_NRESET	Write-only	0x00

Notes: 1. Address value if the MSB mode is activated (see [Section 7.37 on page 38](#)).
2. This register cannot be read if the MSB mode is activated (see [Section 7.37 on page 38](#)).
3. Only in ATSENSE301.

7.1 ADCI0 TAG Register

Name: ADCI0_TAG

Access: Read-only

7	6	5	4	3	2	1	0
–	–	DATA_VALID	TEMPMEAS	TAGI0			

- **TAGI0: TAG of the Anti-tamper ADC Channel**

TAGI0 is equal to 1.

- **TEMPMEAS: Temperature Measurement Status**

0: The external input of the TAMPER ADC is measured.

1: The temperature sensor input of the TAMPER ADC is measured.

- **DATA_VALID: I0 Channel Data Validity Status**

0: The current data is not valid.

1: The current data is valid.

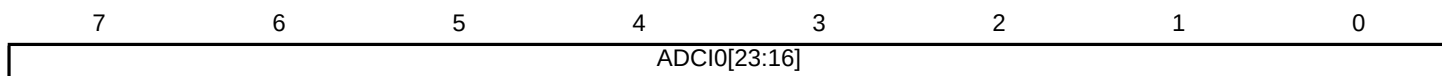
When the source of the ADCI0 channel switches, the decimation filter needs a few samples to stabilize its response (group delay of the filter). Data acquired while DATA_VALID is null are not valid.

This register is not accessible if the MSB_MODE bit is enabled (see [Section 7.37 on page 38](#)).

7.2 ADCI0 Output Bits 23 to 16 Read Register

Name: ADCI0_23_16

Access: Read-only



- **ADCI0_23_16: Bits 23 to 16 of the Anti-tamper ADC Channel**

The address value of this register depends on the value of the MSB_MODE bit (see [Table 7-1 on page 20](#)).

7.3 ADCI0 Output Bits 15 to 8 Read Register

Name: ADCI0_15_8

Access: Read-only



- **ADCI0_15_8: Bits 15 to 8 of the Anti-tamper ADC Channel**

The address value of this register depends on the value of the MSB_MODE bit (see [Table 7-1 on page 20](#)).

7.4 ADCI0 Output Bits 7 to 0 Read Register

Name: ADCI0_7_0

Access: Read-only



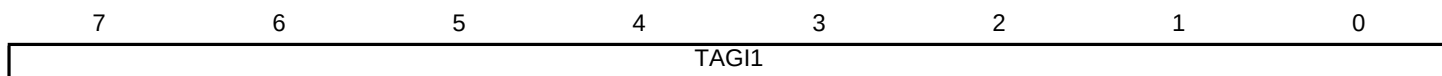
- **ADCI0_7_0: Bits 7 to 0 of the Anti-tamper ADC Channel**

This register is not accessible if the MSB_MODE bit is enabled (see [Section 7.37 on page 38](#)).

7.5 ADCI1 TAG Register

Name: ADCI1_TAG

Access: Read-only



- **TAGI1: TAG of the I1 ADC Channel**

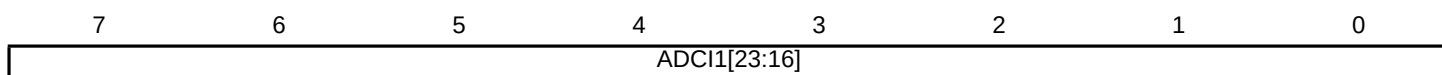
TAGI1 is equal to 2.

This register is not accessible if the MSB_MODE bit is enabled (see [Section 7.37 on page 38](#)).

7.6 ADCI1 Output Bits 23 to 16 Read Register

Name: ADCI1_23_16

Access: Read-only



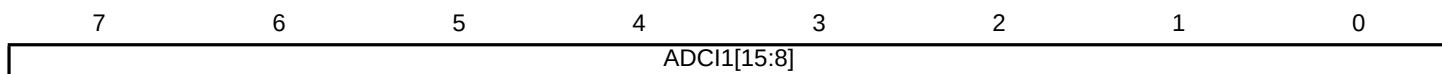
- **ADCI1_23_16: Bits 23 to 16 of the I1 ADC Channel**

The address value of this register depends on the value of the MSB_MODE bit (see [Table 7-1 on page 20](#)).

7.7 ADCI1 Output Bits 15 to 8 Read Register

Name: ADCI1_15_8

Access: Read-only



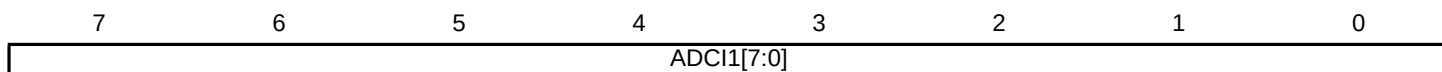
- **ADCI1_15_8: Bits 15 to 8 of the I1 ADC Channel**

The address value of this register depends on the value of the MSB_MODE bit (see [Table 7-1 on page 20](#)).

7.8 ADCI1 Output Bits 7 to 0 Read Register

Name: ADCI1_7_0

Access: Read-only



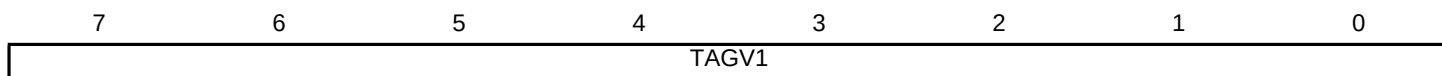
- **ADCI1_7_0: bits 7 to 0 of the I1 ADC channel**

This register is not accessible if the MSB_MODE bit is enabled (see [Section 7.37 on page 38](#)).

7.9 ADCV1 TAG Register

Name: ADCV1_TAG

Access: Read-only



- **TAGV1: TAG of the V1 ADC Channel**

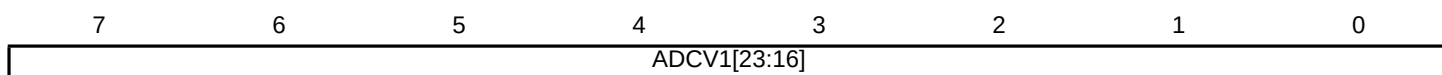
TAGV1 is equal to 3.

This register is not accessible if the MSB_MODE bit is enabled (see [Section 7.37 on page 38](#)).

7.10 ADCV1 Output Bits 23 to 16 Read Register

Name: ADCV1_23_16

Access: Read-only



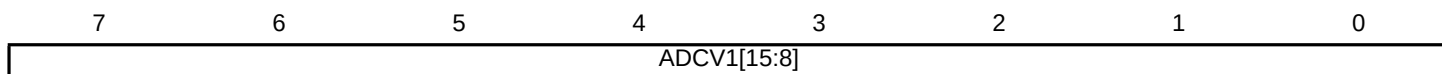
- **ADCV1_23_16: Bits 23 to 16 of the V1 ADC Channel**

The address value of this register depends on the value of the MSB_MODE bit (see [Table 7-1 on page 20](#)).

7.11 ADCV1 Output Bits 15 to 8 Read Register

Name: ADCV1_15_8

Access: Read-only



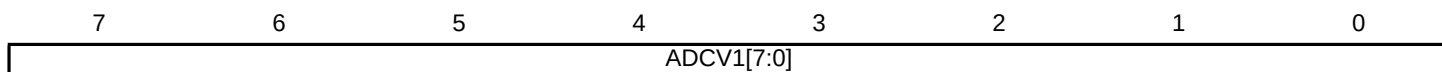
- **ADCV1_15_8: Bits 15 to 8 of the V1 ADC Channel**

The address value of this register depends on the value of the MSB_MODE bit (see [Table 7-1 on page 20](#)).

7.12 ADCV1 Output Bits 7 to 0 Read Register

Name: ADCV1_7_0

Access: Read-only



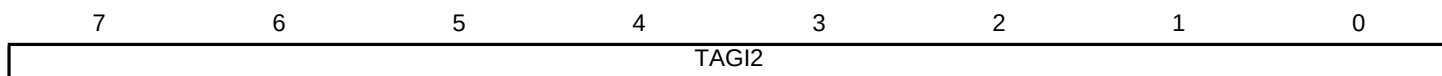
- **ADCV1_7_0: Bits 7 to 0 of the V1 ADC Channel**

This register is not accessible if the MSB_MODE bit is enabled (see [Section 7.37 on page 38](#)).

7.13 ADCI2 TAG Register

Name: ADCI2_TAG

Access: Read-only



- **TAGI2: TAG of the I2 ADC Channel**

TAGI2 is equal to 4.

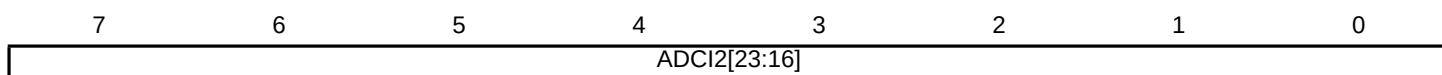
This register is available only in ATSENSE-301(H).

This register is not accessible if the MSB_MODE bit is enabled (see [Section 7.37 on page 38](#)).

7.14 ADCI2 Output Bits 23 to 16 Read Register

Name: ADCI2_23_16

Access: Read-only



- **ADCI2_23_16: Bits 23 to 16 of the I2 ADC Channel**

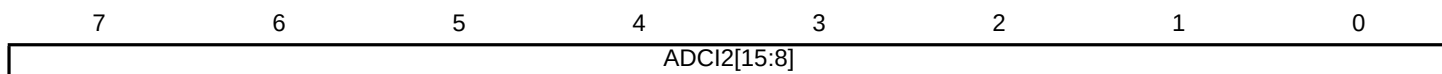
This register is available only in ATSENSE-301(H).

The address value of this register depends on the value of the MSB_MODE bit (see [Table 7-1 on page 20](#)).

7.15 ADCI2 Output Bits 15 to 8 Read Register

Name: ADCI2_15_8

Access: Read-only



- **ADCI2_15_8: Bits 15 to 8 of the I2 ADC Channel**

This register is available only in ATSENSE-301(H).

The address value of this register depends on the value of the MSB_MODE bit (see [Table 7-1 on page 20](#)).

7.16 ADCI2 Output Bits 7 to 0 Read Register

Name: ADCI2_7_0

Access: Read-only



- **ADCI2_7_0: Bits 7 to 0 of the I2 ADC Channel**

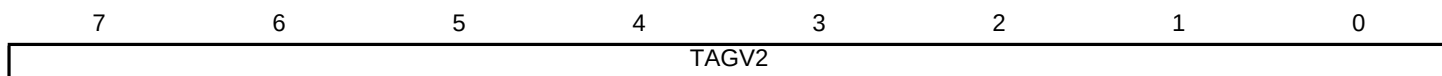
This register is available only in ATSENSE-301(H).

This register is not accessible if the MSB_MODE bit is enabled (see [Section 7.37 on page 38](#)).

7.17 ADCV2 TAG Register

Name: ADCV2_TAG

Access: Read-only



- **TAGV2: TAG of the V2 ADC Channel**

TAGV2 is equal to 5.

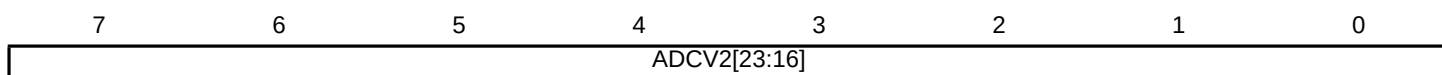
This register is available only in ATSENSE-301(H).

This register is not accessible if the MSB_MODE bit is enabled (see [Section 7.37 on page 38](#)).

7.18 ADCV2 Output Bits 23 to 16 Read Register

Name: ADCV2_23_16

Access: Read-only



- **ADCV2_23_16: Bits 23 to 16 of the V2 ADC Channel**

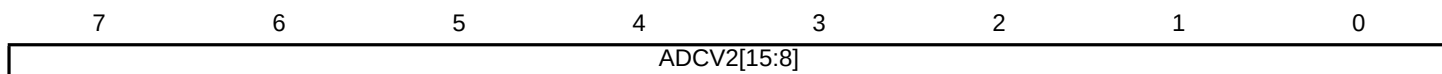
This register is available only in ATSENSE-301(H).

The address value of this register depends on the value of the MSB_MODE bit (see [Table 7-1 on page 20](#)).

7.19 ADCV2 Output Bits 15 to 8 Read Register

Name: ADCV2_15_8

Access: Read-only



- **ADCV2_15_8: Bits 15 to 8 of the V2 ADC Channel**

This register is available only in ATSENSE-301(H).

The address value of this register depends on the value of the MSB_MODE bit (see [Table 7-1 on page 20](#)).

7.20 ADCV2 Output Bits 7 to 0 Read Register

Name: ADCV2_7_0

Access: Read-only



- **ADCV2_7_0: Bits 7 to 0 of the V2 ADC Channel**

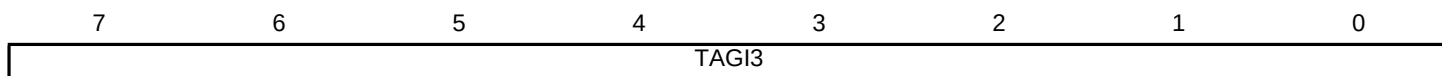
This register is available only in ATSENSE-301(H).

This register is not accessible if the MSB_MODE bit is enabled (see [Section 7.37 on page 38](#)).

7.21 ADCI3 TAG Register

Name: ADCI3_TAG

Access: Read-only



- **TAGI3: TAG of the I3 ADC Channel**

TAGI3 is equal to 6.

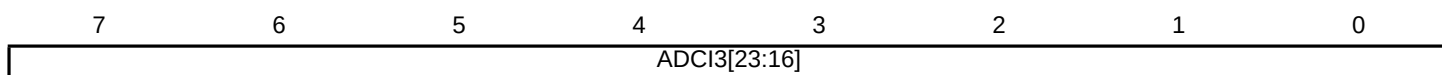
This register is available only in ATSENSE-301(H).

This register is not accessible if the MSB_MODE bit is enabled (see [Section 7.37 on page 38](#)).

7.22 ADCI3 Output Bits 23 to 16 Read Register

Name: ADCI3_23_16

Access: Read-only



- **ADCI3_23_16: Bits 23 to 16 of the I3 ADC Channel**

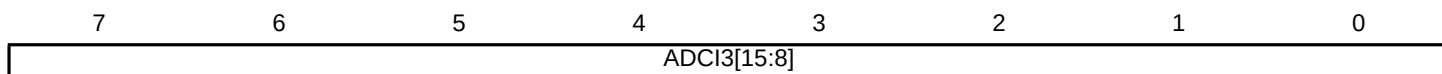
This register is available only in ATSENSE-301(H).

The address value of this register depends on the value of the MSB_MODE bit (see [Table 7-1 on page 20](#)).

7.23 ADCI3 Output Bits 15 to 8 Read Register

Name: ADCI3_15_8

Access: Read-only



- **ADCI3_15_8: Bits 15 to 8 of the I3 ADC Channel**

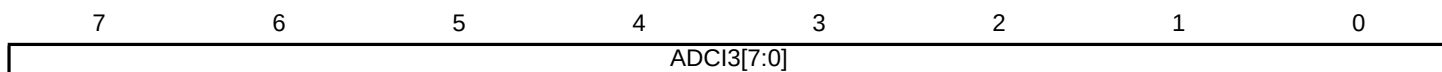
This register is available only in ATSENSE-301(H).

The address value of this register depends on the value of the MSB_MODE bit (see [Table 7-1 on page 20](#)).

7.24 ADCI3 Output Bits 7 to 0 Read Register

Name: ADCI3_7_0

Access: Read-only



- **ADCI3_7_0: Bits 7 to 0 of the I3 ADC Channel**

This register is available only in ATSENSE-301(H).

This register is not accessible if the MSB_MODE bit is enabled (see [Section 7.37 on page 38](#)).

7.25 ADCV3 TAG Register

Name: ADCV3_TAG

Access: Read-only



- **TAGV3: TAG of the V3 ADC Channel**

TAGV3 is equal to 7.

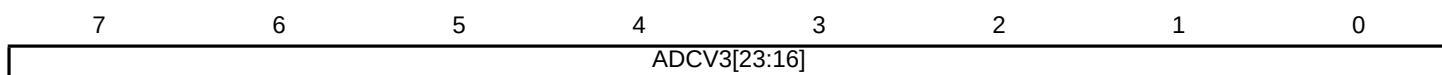
This register is available only in ATSENSE-301(H).

This register is not accessible if the MSB_MODE bit is enabled (see [Section 7.37 on page 38](#)).

7.26 ADCV3 Output Bits 23 to 16 Read Register

Name: ADCV3_23_16

Access: Read-only



- **ADCV3_23_16: Bits 23 to 16 of the V3 ADC Channel**

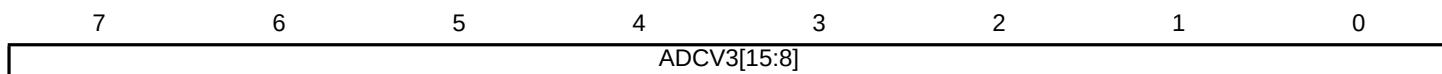
This register is available only in ATSENSE-301(H).

The address value of this register depends on the value of the MSB_MODE bit (see [Table 7-1 on page 20](#)).

7.27 ADCV3 Output Bits 15 to 8 Read Register

Name: ADCV3_15_8

Access: Read-only



- **ADCV3_15_8: Bits 15 to 8 of the V3 ADC Channel**

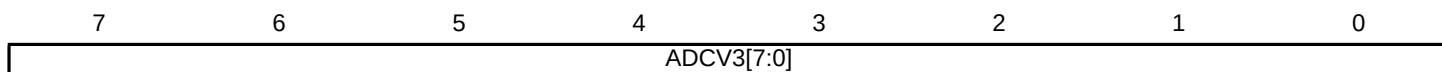
This register is available only in ATSENSE-301(H).

The address value of this register depends on the value of the MSB_MODE bit (see [Table 7-1 on page 20](#)).

7.28 ADCV3 Output Bits 7 to 0 Read Register

Name: ADCV3_7_0

Access: Read-only



- **ADCV3_7_0: Bits 7 to 0 of the V3 ADC Channel**

This register is available only in ATSENSE-301(H).

This register is not accessible if the MSB_MODE bit is enabled (see [Section 7.37 on page 38](#)).

7.29 ADCI0 Controls Register

Name: SDI0

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	GAIN		–	–	TEMPMEAS	ONADC

- **ONADC: ADC Enable**

0: ADC is disabled.

1: ADC is enabled.

When set, this bit can be read at one only after 768 μ s.

- **TEMPMEAS: Temperature Measurement Activation**

0: The external input of the TAMPER ADC is measured.

1: The temperature sensor input of the TAMPER ADC is measured.

This register must not be modified as long as the DATA_VALID bit is low (see “[ADCI0 TAG Register](#)” on page 22).

- **GAIN: Gain Configuration of the ADC**

Value	Name	Description
0	ADC_GAINX1	Input stage of the ADC has a gain of 1
1	ADC_GAINX2	Input stage of the ADC has a gain of 2
2	ADC_GAINX4	Input stage of the ADC has a gain of 4
3	ADC_GAINX8	Input stage of the ADC has a gain of 8

7.30 ADCI1 Controls Register

Name: SDI1

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	GAIN		–	–	–	ONADC

- **ONADC: ADC Enable**

0: ADC is disabled.

1: ADC is enabled.

When set, this bit can be read at one only after 768 μ s.

- **GAIN: Gain Configuration of the ADC**

Value	Name	Description
0	ADC_GAINX1	Input stage of the ADC has a gain of 1
1	ADC_GAINX2	Input stage of the ADC has a gain of 2
2	ADC_GAINX4	Input stage of the ADC has a gain of 4
3	ADC_GAINX8	Input stage of the ADC has a gain of 8

7.31 ADCV1 Controls Register

Name: SDV1

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	ONADC

- **ONADC: ADC Enable**

0: ADC is disabled.

1: ADC is enabled.

When set, this bit can be read at one only after 768 μ s.

7.32 ADCI2 Controls Register

Name: SDI2

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	GAIN		–	–	–	ONADC

This register is available only in ATSENSE-301(H).

- **ONADC: ADC Enable**

0: ADC is disabled.

1: ADC is enabled.

When set, this bit can be read at one only after 768 μ s.

- **GAIN: Gain Configuration of the ADC**

Value	Name	Description
0	ADC_GAINX1	Input stage of the ADC has a gain of 1
1	ADC_GAINX2	Input stage of the ADC has a gain of 2
2	ADC_GAINX4	Input stage of the ADC has a gain of 4
3	ADC_GAINX8	Input stage of the ADC has a gain of 8

7.33 ADCV2 Controls Register

Name: SDV2

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	ONADC

This register is available only in ATSENSE-301(H).

- **ONADC: ADC Enable**

0: ADC is disabled.

1: ADC is enabled.

When set, this bit can be read at one only after 768 μ s.

7.34 ADCI3 Controls Register

Name: SDI3

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	GAIN		–	–	–	ONADC

This register is available only in ATSENSE-301(H).

- **ONADC: ADC Enable**

0: ADC is disabled.

1: ADC is enabled.

When set, this bit can be read at one only after 768 μ s.

- **GAIN: Gain Configuration of the ADC**

Value	Name	Description
0	ADC_GAINX1	Input stage of the ADC has a gain of 1
1	ADC_GAINX2	Input stage of the ADC has a gain of 2
2	ADC_GAINX4	Input stage of the ADC has a gain of 4
3	ADC_GAINX8	Input stage of the ADC has a gain of 8

7.35 ADCV3 Controls Register

Name: SDV3

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	ONADC

This register is available only in ATSENSE-301(H).

- **ONADC: ADC Enable**

0: ADC is disabled.

1: ADC is enabled.

When set, this bit can be read at one only after 768 μ s.

7.36 Analog Controls Register

Name: ANA_CTRL

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	–	–	–	ONLDO	ONREF	ONBIAS

- **ONBIAS: Enable of the Current Bias Generator**

0: The current bias generator is disabled.

1: The current bias generator is enabled.

- **ONREF: Enable of the Voltage Reference**

0: The voltage reference is disabled.

1: The voltage reference is enabled.

When set, this bit can be read at one after 768 μ s.

- **ONLDO: Enable of the Internal LDO**

0: The LDO is disabled.

1: The LDO is enabled.

When set, this bit can be read at one after 928 μ s.

7.37 ATSENSE Configuration Register

Name: ATCFG

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	–	MSB_MODE	–	–	OSR	

- **OSR: OSR of the Decimation Filters**

Value	Name	Description
0	OSR8	OSR of the system is 8
1	OSR16	OSR of the system is 16
2	OSR32	OSR of the system is 32
3	OSR64	OSR of the system is 64

The oversampling ratio (OSR) is the ratio between the input sampling rate F_{Sin} (ADC sampling rate, typically 1.024 MHz) and the output sampling rate F_{Sout} of the decimation filter. .

$$F_{Sout} = \frac{F_{Sin}}{OSR}$$

The OSR must be set before switching on any ADC. Its value must not be changed if any of the ADCs are operating.

- **MSB_MODE: Selection Between 32-bit or 16-bit ADC Mode**

Value	Name	Description
0	32BITS_MODE	The interface sends an 8-bit tag followed by the 24 bits of the ADC conversion (ADCx_TAG, ADCx_23_16, ADCx_15_8 and ADCx_7_0 registers).
1	16BITS_MODE	The interface sends the 16 MSB of the ADC conversion (ADCx_23_16 and ADCx_15_8 registers). The addresses of these registers are modified while ADCx_TAG and ADCx_7_0 are no longer readable.

7.38 ATSENSE Status Register

Name: ATSR

Access: Read-only

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	SYSRDY

- **SYSRDY: System Ready**

0: The system is not ready.

1: The system is ready.

Each time a soft or a hard reset is performed, the system operates initialization operations. ATSR indicates the end of these operations.

While ATSR is not high, no write access is possible in the registers.

7.39 Output Interrupt Line Control Register

Name: ITOUTCR

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	–	–	–	ADC_RDY_OUT	UNDES_OUT	OVRES_OUT

- **OVRES_OUT: Overrun Output Enable**

1: The OVRES interrupt activates the ITOUT output.

0: The OVRES interrupt does not activate the ITOUT output.

- **UNDES_OUT: Underrun Output Enable**

1: The UNDES interrupt activates the ITOUT output.

0: The UNDES interrupt does not activate the ITOUT output.

- **ADC_RDY_OUT: ADC Ready Output Enable**

1: The ADC_RDY interrupt activates the ITOUT output.

0: The ADC_RDY interrupt does not activate the ITOUT output.

7.40 Interrupt Control Register

Name: ITCR

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	–	–	–	ADC_RDY_EN	UNDES_EN	OVRES_EN

- **OVRES_EN: Overrun Interrupt Enable**

0: The generation of the overrun interrupt is disabled.

1: The generation of the overrun interrupt is enabled.

The ovres status generation should be disabled in case of access to data registers through multiple SPI accesses (not simultaneously with the burst mode). In this case, the interrupt is generated as soon as the second access is performed.

- **UNDES_EN: Underrun Interrupt Enable**

0: The generation of the underrun interrupt is disabled.

1: The generation of the underrun interrupt is enabled.

- **ADC_RDY_EN: ADC Ready Interrupt Enable**

0: The generation of the ADC ready interrupt is disabled.

1: The generation of the ADC ready interrupt is enabled.

7.41 Interrupt Status Register

Name: ITSR

Access: Read-only

7	6	5	4	3	2	1	0
–	–	–	–	–	ADC_RDY	UNDES	OVRES

- **OVRES: Overrun Status**

An overrun occurs when the host reads the data registers twice without updating the register values.

The ovres status generation should be disabled if data registers are read by multiple SPI accesses (not at once with the burst mode). In this case, the interrupt will be generated as soon as the second read access is performed.

This register is reset on read.

- **UNDES: Underrun Status**

An underrun occurs when two data register updates occur without read operation.

This register is reset on read.

- **ADC_RDY: ADC Ready Status**

ADC ready interrupt is generated as soon as one ADC conversion is performed.

This register is reset on read.

7.42 Software Reset Register

Name: SOFT_NRESET

Access: Write-only

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	NRESET

- **NRESET: Chip Reset**

When low, the entire chip is in reset state except the SPI interface and the SOFT_NRESET register.

When high, the reset state is released.

8. Software Example

This section details the steps to bring up the ATSENSE-101/ATSENSE-301(H).

1. Power the VDDIO / VDDIN plane with a 3.3V voltage.
2. If internal VDDA regulator is not used, power the VDDA pin with a 2.8V voltage.
3. If internal voltage reference is not used, power the VREF pin with a 1.2V standard voltage reference.
4. Release the internal reset:
 - SPI_WRITE 0x01 @ 0x2D [SOFT_N_RST].
5. If used, start the VDDA regulator:
 - SPI_WRITE 0x04 @ 0x27 [ANACTRL].
6. Start the analog BIAS generator:
 - SPI_WRITE 0x05 @ 0x27.
7. If used, start the voltage reference:
 - SPI_WRITE 0x07 @ 0x27. Wait 100ms to account for VREF settling.
8. Enable the interrupts:
 - SPI_WRITE 0x07 @ 0x2A [ITCR],
9. Enable the Output Interrupt line:
 - SPI_WRITE 0x07 @ 0x2B [ITOUTCR],
10. Start the converters:
 - SPI_WRITE 0x31 @ 0x20 [SDI0], channel I0 ON with gain x8,
 - SPI_WRITE 0x31 @ 0x21 [SDI1], channel I1 ON with gain x8,
 - SPI_WRITE 0x01 @ 0x22 [SDV1], channel V1 ON,
 - SPI_WRITE 0x31 @ 0x23 [SDI2], channel I2 ON with gain x8,⁽¹⁾
 - SPI_WRITE 0x01 @ 0x24 [SDV2], channel V2 ON,⁽¹⁾
 - SPI_WRITE 0x31 @ 0x25 [SDI3], channel I3 ON with gain x8,⁽¹⁾
 - SPI_WRITE 0x01 @ 0x26 [SDV3], channel V3 ON.⁽¹⁾
11. Upon interrupt line ITOUT negative edge, read the ADC conversion results in registers ranging from address 0x00 to 0x1B.

Note: 1. Only for ATSENSE-301(H).

9. Electrical Characteristics

9.1 Absolute Maximum Ratings

Table 9-1. Absolute Maximum Ratings

Operating Temperature (Industrial).....	-40 °C to + 85°C
Storage Temperature.....	-55°C to + 150°C
Power Supply Input on V _{DDIO} , V _{DDIN}	-0.3V to + 4.0V
Digital I/O Input Voltage.....	-0.3V to + 4.0V
Analog Input Voltage on VPx, VN, IPx, INx	-2.0V to + 4.0V
All Other Pins	-0.3V to + 4.0V
Maximum Output Current per pin	100mA
ESD (all pins).....	2 KV HBM ⁽¹⁾

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes: 1. According to specifications MIL-883-Method 3015.7 (HBM - Human Body Model)

9.2 Recommended Operating Conditions

Table 9-2. Recommended Operating Conditions

Parameter	Condition	Min	Max	Units
Operating Ambient Temperature		-40	85	°C
Power Supply Input	V _{DDIO} , V _{DDIN}	3.0	3.6	V
Digital I/O Input Voltage		-0.3	V _{DDIO} + 0.3	V
Analog Inputs Voltage Range	On I _{P{0,1,2,3}} , I _{N{0,1,2,3}} and V _{P{1,2,3}}	-0.25	0.25	V

9.3 Current Consumption

Table 9-3. Current Consumption

Symbol	Parameter	Comments	Min	Typ	Max	Units
I _{DD_OFF}	Device not started.	Master Clock not running. V _{VDDIO} = V _{VDDIN} = 3.3V	–	–	1	µA
I _{DD_ON_k.ADC}	k Channels ON (k≥1), Voltage Reference ON, LDO regulator ON.	Master Clock @ 4.096MHz V _{VDDIO} = V _{VDDIN} = 3.3V	–	1.4 + k * 0.75	1.9 + k * 1.1	mA

9.4 Power-On-Reset Thresholds

Table 9-4. Power-On-Reset Thresholds

Symbol	Parameter	Comments	Min	Typ	Max	Units
V_{T_RISE}	V_{DDIO} Rising Threshold	DC level	2.5	2.6	2.8	V
V_{T_FALL}	V_{DDIO} Falling Threshold	DC level	2.35	2.5	2.65	V
V_{T_HYST}	$V_{T_RISE} - V_{T_FALL}$		90	120	180	mV

9.5 Digital I/Os DC Characteristics

Table 9-5. Digital I/Os Characteristics

Symbol	Parameter	Comments	Min	Typ	Max	Units
V_{DDIO}	Operating Supply Voltage		3.0	–	3.6	V
V_{IL}	Input Low-Level Voltage		-0.3	–	$0.3 \times V_{DDIO}$	V
V_{IH}	Input High-Level Voltage		$0.7 \times V_{DDIO}$	–	$V_{DDIO} + 0.3$	V
V_{OL}	Output Low-Level Voltage	I_O max.	–	–	$0.25 \times V_{DDIO}$	V
V_{OH}	Output Low-Level Voltage	I_O max.	$0.75 \times V_{DDIO}$	–	–	V
I_O	Output Current (sink or source)		–	–	8	mA

9.6 Measurement Channels

Unless otherwise specified: External components according to [Section 3. "Application Block Diagram"](#): $C_{VREF}=1\mu F$ and $C_{VDDA}=1\mu F$, $MCLK = 4.096MHz$, $V_{DDIN} = V_{DDIO} = 3.3V$, Noise Bandwidth = [30Hz, 2kHz], $T_J = [-40^{\circ}C ; +100^{\circ}C]$.

Table 9-6. Measurement Channel Electrical Characteristics

Symbol	Parameter	Comments	Min	Typ	Max	Units
V_{VDDA}	Operating Supply Voltage		2.7	2.8	2.9	V
I_{VDD}	Channel Supply Current ⁽¹⁾ in VDDIO and VDDA	OFF	–	–	1	μA
		ON	–	0.75	1	mA
F_{MCLK}	Master Clock Input Frequency		3.9	4.096	4.3	MHz
$Duty_{MCLK}$	Master Clock Input Duty Cycle		48	–	52	%
V_{IND_FS}	A/D Converter Input Referred Full Scale Voltage ⁽²⁾	$V_{REF} = 1.2V$ $V_{IND} = V_{VPX}$ or $V_{IND} = V_{IPX} - V_{INX}$ G: Channel Gain = {1, 2, 4 or 8}	–	1.2 / G	–	V_{PP}
V_{CM_IN}	Common Mode Input Voltage Range	$(V_{IPX} + V_{INX}) / 2$	-20	–	20	mV
Z_{IN0}	Common Mode Input Impedance at $T_{J0} = 23^{\circ}C$	G: Channel Gain = {1, 2, 4 or 8} On V_{PX} , V_{IPX} , V_{INX} pins. $F_{MCLK} = 4.096$ MHz	400 / G	480 / G	560 / G	k Ω
$SINAD_{PEAK}$	Peak Signal to Noise and Distortion Ratio $F_{IN} = 45$ to $66Hz$ $BW = [30Hz, 2kHz]$	Gain = 1, $V_{IND} = 1.000 V_{PP}$	–	84	–	dB
		Gain = 2, $V_{IND} = 0.500 V_{PP}$	–	84	–	
		Gain = 4, $V_{IND} = 0.250 V_{PP}$	–	82	–	
		Gain = 8, $V_{IND} = 0.125 V_{PP}$	–	81	–	
E_N	Input Referred Noise Voltage integrated over [30Hz, 2kHz]	Gain = 1	–	21	–	μV_{RMS}
		Gain = 2	–	10	–	
		Gain = 4	–	6	–	
		Gain = 8	–	3.3	–	
S_N	Input Referred Noise Voltage Density at fundamental frequency. (Between 45 and 66Hz).	Gain = 1	–	470	–	nV/ $\sqrt{Hz}$
		Gain = 2	–	220	–	
		Gain = 4	–	130	–	
		Gain = 8	–	73	–	
EG_0	Gain Error	$T_{J0} = 23^{\circ}C$. $V_{REF} = 1.2V$	-3		3	%
TC_G	Channel Gain drift with temperature ⁽³⁾	$-40^{\circ}C < T_J < 100^{\circ}C$, $V_{REF} = 1.2V$ $R_{SOURCE} = 3k\Omega$	–	-5	–	ppm/ $^{\circ}C$
V_{OS0}	Input Referred Offset	$T_{J0} = 23^{\circ}C$	-5 / G	–	5 / G	mV
TC_{VOS}	V_{OS} drift with temperature	$-40^{\circ}C < T_J < 100^{\circ}C$	-2	–	+2	$\mu V/^{\circ}C$

Notes: 1. Current consumption per measurement channel.

2. V_{IND} may be limited by the recommended input voltage on analog input pins (+/-0.25V, See [Table 9-2, "Recommended Operating Conditions"](#)).

3. Includes the input impedance drift with temperature.

9.7 Voltage Reference and Die Temperature Sensor

Unless otherwise specified: External components according to [Section 3. "Application Block Diagram"](#): $C_{VREF}=1\mu F$ and $C_{VDDA}=1\mu F$, $MCLK = 4.096MHz$, $V_{DDIN} = V_{DDIO} = 3.3V$, $T_J = [-40^{\circ}C; +100^{\circ}C]$.

Table 9-7. Voltage Reference and Die Temperature Sensor Electrical Characteristics

Symbol	Parameter	Comments	Min	Typ	Max	Units
V_{VDPA}	Operating Supply Voltage		2.7	2.8	2.9	V
I_{VDPA}	Supply Current	OFF	–	–	0.1	μA
		ON	–	70	100	
V_{REF0}	Output voltage initial accuracy	At $T_{J0} = 23^{\circ}C$	1.142	1.144	1.146	V
TC_{VREF_U}	V_{REF} drift with temperature ⁽¹⁾	Uncompensated	–	50	–	ppm/ $^{\circ}C$
TC_{VREF_C}		Using factory programmed calibration registers.	–	10	–	
R_{OUT}	V_{REF} output resistance		200	500	800	Ω
D_{TEMP_Lin}	Die Temperature Sensor, Digital Reading Linearity		–	+/-2	–	$^{\circ}C$
I_{VREF_OFF}	Current in VREF pin when internal voltage reference is OFF		-100	–	100	nA

Note: 1. TC is defined using the box method: $TC = (V_{REF_MAX} - V_{REF_MIN}) / (V_{REF0} \times (T_{MAX} - T_{MIN}))$

9.8 VDDA LDO Regulator

Unless otherwise specified: External components according to [Section 3. "Application Block Diagram"](#): $C_{VREF}=1\mu F$ and $C_{VDPA}=1\mu F$, $MCLK = 4.096MHz$, $V_{DDIN} = V_{DDIO} = 3.3V$, $T_J = [-40^{\circ}C; +100^{\circ}C]$.

Table 9-8. VDDA LDO regulator

Symbol	Parameter	Comments	Min	Typ	Max	Units
V_{VDDIN}	Operating Supply Voltage		3.0	3.3	3.6	V
I_{VDDIN}	Supply Current	OFF	–	–	0.1	μA
		ON	–	–	250	
I_O	Output Current		–	–	15	mA
V_O	DC Output Voltage	$I_O = 0mA$.	2.75	2.8V	2.85	V
$\Delta V_O / \Delta I_O$	Static Load Regulation	I_O 0 to I_{OMAX}	–	–	-35	mV
$\Delta V_O / \Delta V_{DDIN}$	Static Line Regulation	V_{DDIN} : 3.0 to 3.6V	–	1	5	mV
PSRR	Power Supply Rejection Ratio	$f = DC$ to 2000 Hz	–	40	–	dB
		$f = 1$ MHz	–	50	–	
T_{START}	Start-Up time	V_O from 0 to 95% of final value. $I_O = 0mA$.	–	–	1	ms
C_O	Stable Output Capacitor Range	Capacitive	0.5	1	4.7	μF
		Resistive	5	10	300	m Ω

10. Mechanical Characteristics

Figure 10-1. 20-lead SOIC Package

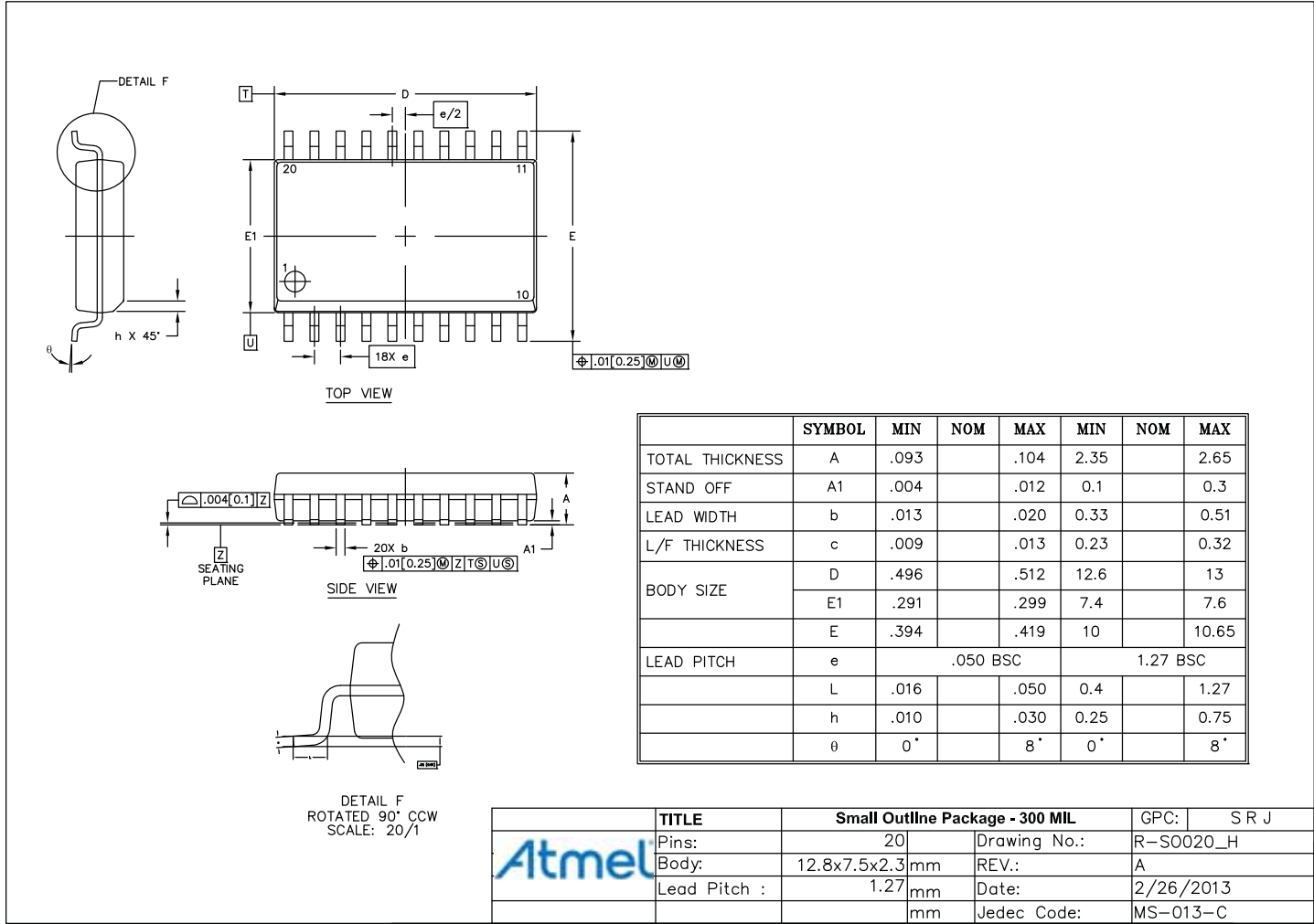
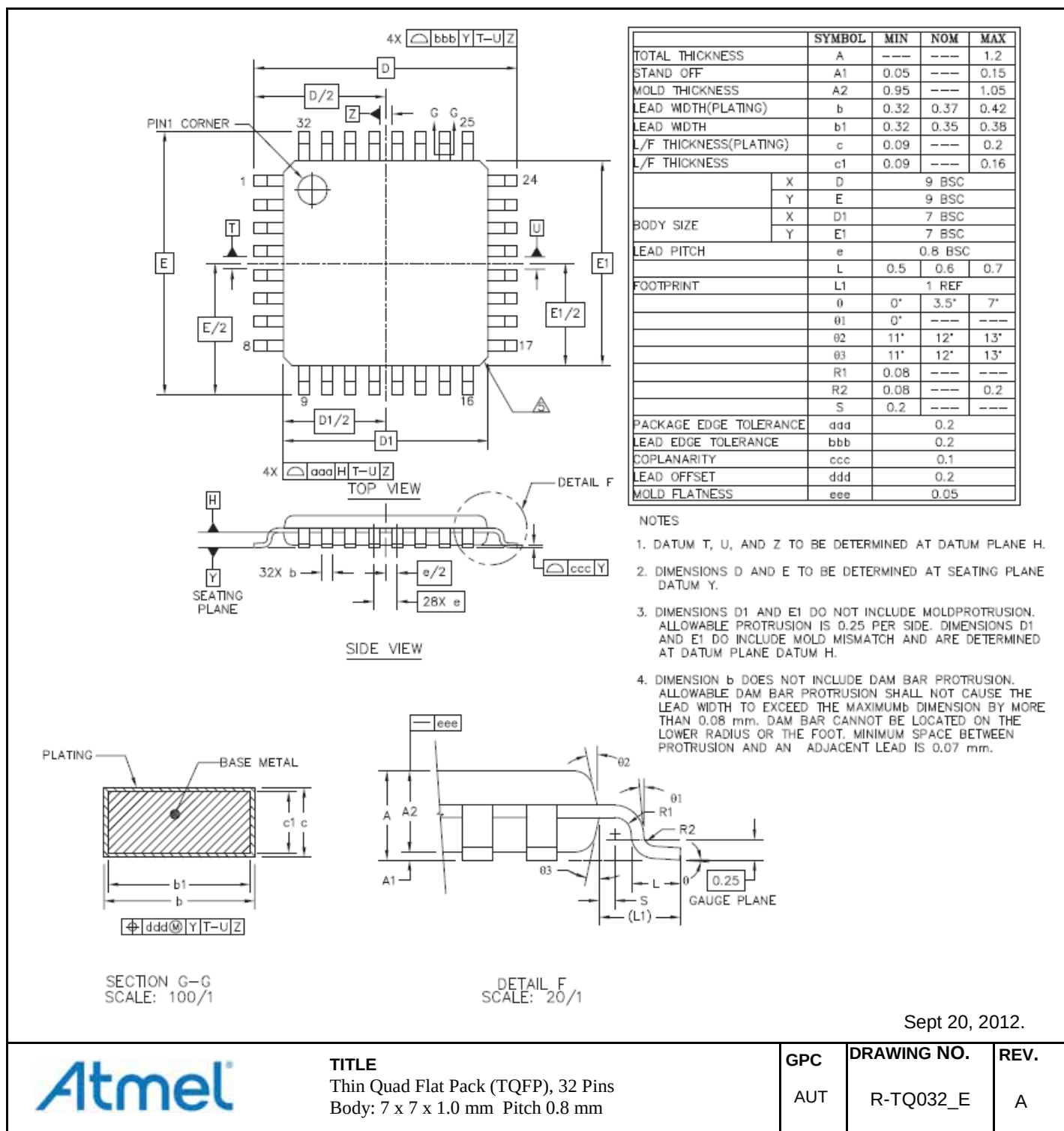


Figure 10-2. 32-lead TQFP Package



11. Ordering Information

Ordering Code	Package	Carrier Type	Package Type	Temperature Operating Range
ATSENSE101A-SU	SOIC20		Green	Industrial (-40°C to +85°C)
ATSENSE301A-AUR	TQFP32	Tape & Reel	Green	
ATSENSE301HA-AUR				

12. Revision History

In the table that follows, the most recent version of the document appears first.

“rfo” indicates changes requested during document review and approval loop.

Doc. Rev.	Comments	Change Request Ref.
11219A		
	First Issue	

Table of Contents

Description	1
Features	1
1. Block Diagrams	2
2. Package and Pinout	4
2.1 ATSENSE-301(H)	4
2.2 ATSENSE-101	6
3. Application Block Diagram	7
4. Functional Description	9
4.1 Conversion Channels	9
4.2 Voltage Reference, Die Temperature Measurement and Calibration Registers	10
4.3 Voltage Reference Value at TL: MSB	12
4.4 Voltage Reference Value at TL: LSB	12
4.5 Temperature Sensor Value at TL: MSB	13
4.6 Temperature Sensor Value at TL: LSB	13
4.7 Voltage Reference Value at TH: MSB	14
4.8 Voltage Reference Value at TH: LSB	14
4.9 Temperature Sensor Value at TH: MSB	15
4.10 Temperature Sensor Value at TH: LSB	15
4.11 Correction Algorithm	16
5. SPI Controller	17
5.1 Description	17
5.2 SPI Serial Port	17
6. Interrupt Controller	19
6.1 ADC Ready	19
6.2 Overrun	19
6.3 Underrun	19
7. SPI Controller User Interface	20
7.1 ADCI0 TAG Register	22
7.2 ADCI0 Output Bits 23 to 16 Read Register	23
7.3 ADCI0 Output Bits 15 to 8 Read Register	23
7.4 ADCI0 Output Bits 7 to 0 Read Register	23
7.5 ADCI1 TAG Register	24
7.6 ADCI1 Output Bits 23 to 16 Read Register	24
7.7 ADCI1 Output Bits 15 to 8 Read Register	24
7.8 ADCI1 Output Bits 7 to 0 Read Register	24
7.9 ADCV1 TAG Register	25
7.10 ADCV1 Output Bits 23 to 16 Read Register	25
7.11 ADCV1 Output Bits 15 to 8 Read Register	25
7.12 ADCV1 Output Bits 7 to 0 Read Register	25
7.13 ADCI2 TAG Register	26
7.14 ADCI2 Output Bits 23 to 16 Read Register	26
7.15 ADCI2 Output Bits 15 to 8 Read Register	26
7.16 ADCI2 Output Bits 7 to 0 Read Register	26

7.17	ADCV2 TAG Register	27
7.18	ADCV2 Output Bits 23 to 16 Read Register	27
7.19	ADCV2 Output Bits 15 to 8 Read Register	27
7.20	ADCV2 Output Bits 7 to 0 Read Register	27
7.21	ADCI3 TAG Register	28
7.22	ADCI3 Output Bits 23 to 16 Read Register	28
7.23	ADCI3 Output Bits 15 to 8 Read Register	28
7.24	ADCI3 Output Bits 7 to 0 Read Register	28
7.25	ADCV3 TAG Register	29
7.26	ADCV3 Output Bits 23 to 16 Read Register	29
7.27	ADCV3 Output Bits 15 to 8 Read Register	29
7.28	ADCV3 Output Bits 7 to 0 Read Register	29
7.29	ADCI0 Controls Register	30
7.30	ADCI1 Controls Register	31
7.31	ADCV1 Controls Register	32
7.32	ADCI2 Controls Register	33
7.33	ADCV2 Controls Register	34
7.34	ADCI3 Controls Register	35
7.35	ADCV3 Controls Register	36
7.36	Analog Controls Register	37
7.37	ATSENSE Configuration Register	38
7.38	ATSENSE Status Register	39
7.39	Output Interrupt Line Control Register	40
7.40	Interrupt Control Register	41
7.41	Interrupt Status Register	42
7.42	Software Reset Register	43
8.	Software Example	44
9.	Electrical Characteristics	45
9.1	Absolute Maximum Ratings	45
9.2	Recommended Operating Conditions	45
9.3	Current Consumption	45
9.4	Power-On-Reset Thresholds	46
9.5	Digital I/Os DC Characteristics	46
9.6	Measurement Channels	47
9.7	Voltage Reference and Die Temperature Sensor	48
9.8	VDDA LDO Regulator	48
10.	Mechanical Characteristics	49
11.	Ordering Information	51
12.	Revision History	52
	Table of Contents	53



Enabling Unlimited Possibilities®

Atmel Corporation

1600 Technology Drive
San Jose, CA 95110
USA

Tel: (+1) (408) 441-0311

Fax: (+1) (408) 487-2600

www.atmel.com

Atmel Asia Limited

Unit 01-5 & 16, 19F
BEA Tower, Millennium City 5
418 Kwun Tong Road

Kwun Tong, Kowloon

HONG KONG

Tel: (+852) 2245-6100

Fax: (+852) 2722-1369

Atmel Munich GmbH

Business Campus
Parking 4
D-85748 Garching b. Munich

GERMANY

Tel: (+49) 89-31970-0

Fax: (+49) 89-3194621

Atmel Japan G.K.

16F Shin-Osaki Kangyo Bldg
1-6-4 Osaki, Shinagawa-ku
Tokyo 141-0032

JAPAN

Tel: (+81) (3) 6417-0300

Fax: (+81) (3) 6417-0370

© 2013 Atmel Corporation. All rights reserved. / Rev.: 11219A-ATSENSE-15-Oct-13

Atmel®, Atmel logo and combinations thereof, Enabling Unlimited Possibilities® and others are registered trademarks or trademarks of Atmel Corporation or its subsidiaries. Cortex® is a registered trademark of ARM Ltd. Other terms and product names may be trademarks of others.

Disclaimer: The information in this document is provided in connection with Atmel products. No license, express or implied, by estoppel or otherwise, to any intellectual property right is granted by this document or in connection with the sale of Atmel products. EXCEPT AS SET FORTH IN THE ATMEL TERMS AND CONDITIONS OF SALES LOCATED ON THE ATMEL WEBSITE, ATMEL ASSUMES NO LIABILITY WHATSOEVER AND DISCLAIMS ANY EXPRESS, IMPLIED OR STATUTORY WARRANTY RELATING TO ITS PRODUCTS INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. IN NO EVENT SHALL ATMEL BE LIABLE FOR ANY DIRECT, INDIRECT, CONSEQUENTIAL, PUNITIVE, SPECIAL OR INCIDENTAL DAMAGES (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS AND PROFITS, BUSINESS INTERRUPTION, OR LOSS OF INFORMATION) ARISING OUT OF THE USE OR INABILITY TO USE THIS DOCUMENT, EVEN IF ATMEL HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. Atmel makes no representations or warranties with respect to the accuracy or completeness of the contents of this document and reserves the right to make changes to specifications and products descriptions at any time without notice. Atmel does not make any commitment to update the information contained herein. Unless specifically provided otherwise, Atmel products are not suitable for, and shall not be used in, automotive applications. Atmel products are not intended, authorized, or warranted for use as components in applications intended to support or sustain life.