Single Output Controller with SVID Interface for Desktop and Notebook CPU Applications

NCP81283

The NCP81283 (6 phase) is a single rail, six−output buck solution optimized for Intel®'s IMVP9 CPUs. The multi−phase rail control system is based on Dual−Edge pulse−width modulation (PWM) combined with DCR current sensing. This provides an ultra−fast initial response to dynamic load events and reduced system cost. The NCP81283 has an ultra−low offset current monitor amplifier with programmable offset compensation for high accuracy current monitoring.

Multi−Phase Features

- Vin range 4.5 V to 21 V
- Startup into Pre−Charged Loads While Avoiding False OVP
- Digital Soft Start Ramp
- Adjustable Vboot
- High Impedance Differential Output Voltage Amplifiers
- Programmable Output Voltage Slew Rates
- Dynamic VID Feed−Forward
- Differential Current Sense Amplifiers for Each Phase
- Programmable Adaptive Voltage Positioning (AVP)
- Adjustable Switching Frequency Range
- Digitally Stabilized Switching Frequency
- UltraSonic Operation
- This is a Pb−Free Device

Applications

- Desktop & Notebook Processors
- Gaming

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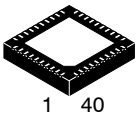
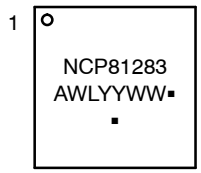


QFN40
CASE 485CR

MARKING DIAGRAM



NCP81283 = Specific Device Code
A = Assembly Site
WL = Wafer Lot Number
YY = Year of Production
WW = Work Week Number
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NCP81283MNTXG	QFN40 (Pb−Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

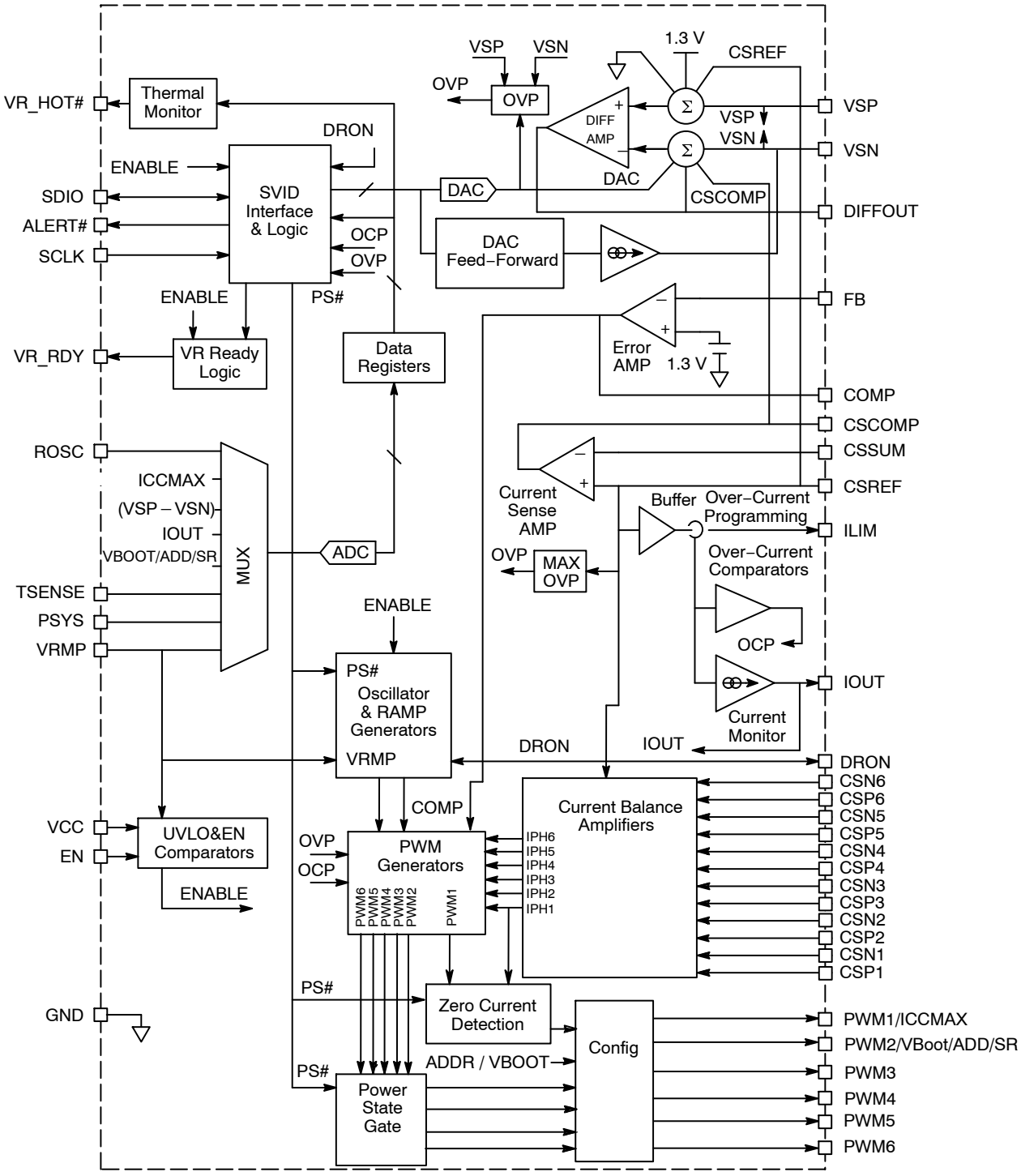


Figure 1. Internal Block Diagram

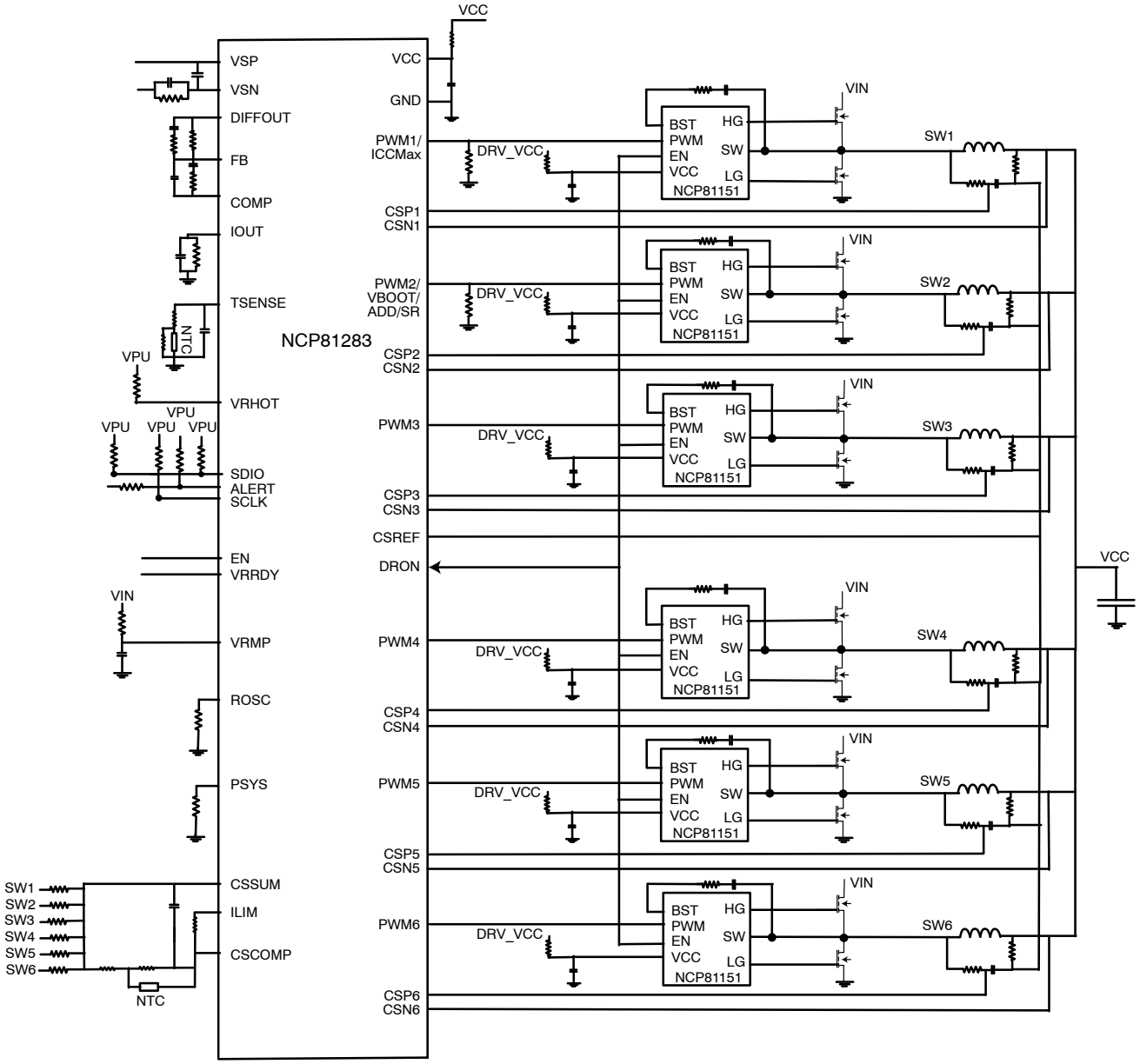


Figure 2. Application Block Diagram

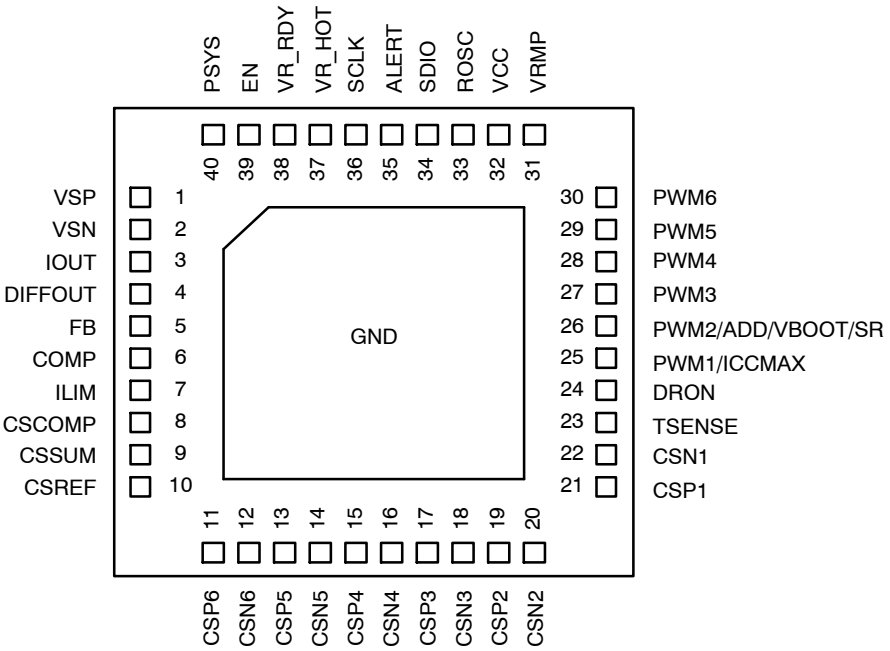


Figure 3. Pinout

PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	VSP	Differential output voltage sense positive
2	VSN	Differential output voltage sense negative
3	IOUT	A resistor to ground programs IOUT gain
4	DIFFOUT	Output of differential remote sense amplifier
5	FB	Error amplifier voltage feedback
6	COMP	Error amplifier output and PWM comparator inverting input
7	ILIM	A resistor to CSCOMP_2PH_A programs the over−current threshold
8	CSCOMP	Total−current−sense amplifier output
9	CSSUM	Inverting input of total−current−sense amplifier
10	CSREF	Total−current−sense amplifier reference voltage input
11	CSP6	Current−balance amplifier positive input for Phase 6
12	CSN6	Non−inverting input to current balance sense amplifier for Phase 6
13	CSP5	Current−balance amplifier positive input for Phase 5
14	CSN5	Non−inverting input to current balance sense amplifier for Phase 5
15	CSP4	Current−balance amplifier positive input for Phase 4
16	CSN4	Non−inverting input to current balance sense amplifier for Phase 4
17	CSP3	Current−balance amplifier positive input for Phase 3
18	CSN3	Non−inverting input to current balance sense amplifier for Phase 3
19	CSP2	Current−balance amplifier positive input for Phase 2
20	CSN2	Non−inverting input to current balance sense amplifier for Phase 2
21	CSP1	Current−balance amplifier positive input for Phase 1
22	CSN1	Non−inverting input to current balance sense amplifier for Phase 1

PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Description
23	TSENSE	Temperature sense input, thermistor should be placed by L1 on board
24	DRON	External FET driver enable for discrete driver or DrMOS
25	PWM1/ICCMAX	Phase 1 PWM output to power stage A resistor to ground programs ICCMAX
26	PWM2/ADD/VBOOT/SR	Phase 2 PWM output to power stage A resistor to ground configures SVID addresses, Vboot and Vout Slew Rate
27	PWM3	Phase 3 PWM output to power stage
28	PWM4	Phase 4 PWM output to power stage
29	PWM5	Phase 5 PWM output to power stage
30	PWM6	Phase 6 PWM output to power stage
31	VRMP	Vin feed−forward input. Controls a current used to generate the ramps of the modulators
32	VCC	Power for the internal control circuits. A decoupling capacitor is connected from this pin to ground
33	ROSC	A resistor to ground configures Switching frequency of the regulator
34	SDIO	Serial VID data interface
35	ALERT#	Serial VID ALERT#
36	SCLK	Serial VID clock
37	VR_HOT#	Thermal logic output for over−temperature condition on TTSENSE pins
38	VR_RDY	VR_RDY indicates all three rails are ready to accept SVID commands
39	EN	Enable input. High enables
40	PSYS	System power monitor input, a 20K resistor to ground is required for PSYS monitoring
41	Tab	GND

MAXIMUM RATINGS (Note 1)

Pin Symbol	VMAX	VMIN	ISOURCE	ISINK
COMP_MPH	VCC + 0.3 V	−0.3 V	2 mA	2 mA
CSCOMP_MPH	VCC + 0.3 V	−0.3 V	2 mA	2 mA
PWMX	VCC + 0.3 V	−0.3 V		1 mA
VSN_MPH	GND + 0.3 V	GND − 0.3 V	1 mA	2 mA
DIFFOUT_MPH	VCC + 0.3 V	−0.3 V	2 mA	2 mA
VR_RDY	VCC + 0.3 V	−0.3 V	2 mA	
VCC	6.0 V	−0.3 V		
VRMP	25 V	−0.3 V		
SCLK, SDIO	3.6 V			
All Other Pins	VCC + 0.3 V	−0.3 V		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All signals referenced to GND unless noted otherwise.

THERMAL CHARACTERISTICS

Description	Symbol	Typ	Unit
Thermal Characteristic QFN Package (Note 2)	RJA	68	°C/W
Operating Junction Temperature Range (Note 3)	TJ	−40 to 125	°C
Operating Ambient Temperature Range		−40 to 100	°C
Maximum Storage Temperature Range	TSTG	−40 to +150	°C
Moisture Sensitivity Level QFN Package	MSL	1	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
2. JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM.
3. JESD 51−7 (1S2P Direct−Attach Method) with 0 LF.

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Min	Max	Unit
VCC Voltage Range	VCC	4.75	5.25	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

($-40°C < T_A < 100°C$; $4.75\ V < V_{CC} < 5.25\ V$; $C_{VCC} = 0.1\ \mu F$ unless otherwise noted)

Characteristic	Test Conditions	Min	Typ	Max	Unit
BIAS SUPPLY					
VCC Voltage Range		4.75		5.25	V
Quiescent Current	PS0		36		mA
	PS1		24		mA
	PS2		20	26	mA
	PS3		13	15	mA
	PS4		70	100	μA
	enable low		34		μA
UVLO Threshold	VCC rising			4.6	V
	VCC falling	3.9			V
UVLO Threshold	VRAMP rising			4.25	V
	VRAMP falling	3.0			V
ENABLE INPUT					
Upper Threshold	Activation Level	0.8			V
Lower Threshold	Deactivation Level			0.3	V
PHASE DETECTION					
CSP Pin Pulldown Current	Pulldown applied only prior to soft start		10		μA
CSP Pin Threshold Voltage		Vcc−0.4			V
Phase Detect Timer			1.75		ms
DAC SLEW RATE					
Soft Start Slew Rate			1/4 fast		mV/μs
Slew Rate Slow			1/4 fast		mV/μs
Slew Rate Fast			48		mV/μs
DRON					
Output High Voltage	Sourcing 500 μA	3			V
Output Low Voltage	Sinking 500 μA			0.1	V
TSENSE					
Bias Current		115	120	125	μA
Alert# Assert Threshold			488		mV

ELECTRICAL CHARACTERISTICS (continued)
($-40°C < T_A < 100°C$; $4.75\ V < V_{CC} < 5.25\ V$; $C_{VCC} = 0.1\ \mu F$ unless otherwise noted)

Characteristic	Test Conditions	Min	Typ	Max	Unit
TSENSE					
Alert# De−Assert Threshold			510		mV
VR_Hot Assert Threshold			468		mV
VR_Hot De−Assert Threshold			488		mV
VR_RDY OUTPUT					
Output Low Saturation Voltage	IVR_RDY = −4 mA		0.3		V
Rise Time	1 kΩ pull−up to 3.3 V		110		ns
Fall Time	CTOT = 45 pF		20		ns
OVP AND UVP					
Absolute Over Voltage Threshold	During Soft Start		3.4		V
Over Voltage Threshold Above DAC	VSP−VSN−VID Rising	360	400	440	mV
Over Voltage Delay	VSP−VSN Rising to PWM Low		25		ns
Under Voltage Threshold Below DAC	VSP−VSN−VID Falling		300		mV
Under Voltage Delay			5		μs
PWM POWER					
Output High Voltage	Sourcing 500 μA	Vcc−0.2			V
Output Mid Voltage	No Load, Power State 2	1.7	1.8	1.9	V
Output Low Voltage	Sinking 500 μA			0.7	V
DIFFERENTIAL SUMMING AMPLIFIER					
Input Bias Current	VSP = VSN = 1.3 V	−25		25	nA
−3dB Bandwidth	CL = 20 pF, RL = 10 kΩ		22.5		MHz
Closed Loop DC Gain	VSP − VSN = 0.5 V to 1.3 V		1		V/V
ERROR AMPLIFIER					
Input Bias Current	@1.3 V	−400		400	nA
Open Loop DC Gain	CL = 20 pF, RL = 10 kΩ		80		dB
Open Loop Unity Gain Bandwidth	CL = 20 pF, RL = 10 kΩ		20		MHz
Slew Rate	ΔVin = 100 mV, G = −10 V/V ΔVout = 1.5 V to 2.5 V, CL = 20 pF, RL = 10 kΩ		5		V/μs
Maximum Output Voltage	ISOURCE = 2.0 mA	4			V
Minimum Output Voltage	ISINK = 2.0 mA			0.9	V
CURRENT SUMMING AMPLIFIER					
Input Bias Current	CSSUM = CSREF = 1.0 V	−8		8	μA
Offset Voltage (Vos)		−500		500	μV
Open Loop Gain			80		dB
Open Loop Unity Gain Bandwidth	CL = 20 pF, RL = 10 kΩ		10		MHz
CURRENT BALANCE AMPLIFIERS					
Differential Mode input Voltage Range	CSREF = 1.2 V	−100		100	mV
−3dB Bandwidth			6		MHz
OVER−CURRENT PROTECTION					
ILim Threshold Current (delayed OCP shutdown)	PS0	9	10	11	μA
	PS1, PS2, PS3		10/N*		μA
ILim Threshold Current (immediate OCP shutdown)	PS0	13.5	15	16.5	μA
	PS1, PS2, PS3		15/N*		μA
Shutdown Delay	Immediate		300		ns
	Delayed		50		μs
ILim Output Voltage Offset	ILim sourcing 15 μA	−3		3	mV

*N is the phase configuration number in PS0.

ELECTRICAL CHARACTERISTICS (continued)
($-40°C < T_A < 100°C$; $4.75\ V < V_{CC} < 5.25\ V$; $C_{VCC} = 0.1\ \mu F$ unless otherwise noted)

Characteristic	Test Conditions	Min	Typ	Max	Unit
IOUT OUTPUT					
Output Offset Current	ILimit to CSREF			0.25	μA
Current Gain	IOUT/ILIM, (RLIM = 20 kΩ, RIOUT = 5 Ω) DAC = 0.8 V, 1.25 V, 1.5 V	9.5	10	10.5	A/A
MODULATORS					
PWM Ramp Duty Cycle Matching	Comp = 2 V, PWM Ton Matching		±3		%

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

START UP

Following the rise of VCC above the UVLO threshold, externally programmed configuration data is collected, and all PWM outputs are set to Mid−level to prepare the gate drivers of the power stages for activation. When the controller is enabled, DRON is asserted (high) to activate the external gate drivers. A digital counter steps the DAC up from zero to the target boot voltage based on the Soft Start Slew Rate in the spec table. As the DAC ramps, the PWM outputs of each rail will change from Mid−level to high when the first PWM pulse for that rail is produced.

When the controller is disabled, the PWM signals return to Mid−level.

DEVICE CONFIGURATION

Phase and Rail Configuration

During start−up, the number of operational phases of the multiphase rail is determined by the internal circuitry monitoring the CSP inputs. If a reduced phase count is required the appropriate CSP pins externally pulled to VCC with a resistor during startup.

NCP81283 Configurations

The NCP81283 has four Configuration features. On power up a 10 μA current is sourced from these pins through a resistor connected to these pins (pins 26 and 33) and the resulting voltage is measured. The following features will be programmed:

- Serial VID Address
- Slew Rate
  - Programs the slew rate of VBOOT on power up
- ROSC (Switching Frequency)
  - The Fsw values are shown in Table 1
- Vboot
  - Vboot options are shown in Table 2

Switching Frequency

Switching frequencies between 220 kHz and 1.2 MHz are programmed at startup with pulldown resistors on Rosc pin (please see pinout for pin number).

Table 1. SWITCHING FREQUENCY

Resistor (kΩ)	Switching Frequency
10	1.2 MHz
14.7	1.1 MHz
20	1.0 MHz
26.1	900 kHz
33.2	850 kHz
41.2	800 kHz
49.9	750 kHz
60.4	700 kHz
71.5	650 kHz
84.5	600 kHz
100	550 kHz
118.3	500 kHz
136.6	450 kHz
157.7	400 kHz
182.1	300 kHz
249	200 kHz

Table 2. SERIAL VID ADDRESS, VBOOT AND SLEW RATE

Level	Resistor (kΩ)	ADD	SR	Vboot
1	10	0	10	0
2	14.7	1	10	0
3	20	2	10	0
4	26.1	0	48	0
5	33.2	1	48	0
6	41.2	2	48	0
7	49.9	0	30	0
8	60.4	1	30	0
9	71.5	0	10	1.8
10	84.5	1	10	1.8
11	100	2	10	1.8
12	118.3	0	48	1.8
13	136.6	1	48	1.8
14	157.7	2	48	1.8
15	182.1	0	30	1.8
16	249	1	30	1.8

ICCMAX

A resistor to ground on the ICCMAX pin programs these registers at the time the part is enabled. 10 μA is sourced from these pins to generate a voltage on the program resistor. The resistor value should be no less than 10 kΩ.

$$ICC\_MAX_{21h} = \frac{R \cdot 10\ \mu A \cdot 256\ A}{2\ V} \qquad \text{(eq. 1)}$$

Ultrasonic Mode

The switching frequency of a rail in DCM will decrease at very light loads. Ultrasonic Mode forces the switching frequency to stay above the audible range.

CCM/DCM Operation

In PS2 and PS3, all rails will operate in either Continuous Conduction Mode (CCM) or discontinuous Conduction Mode (DCM) depending on load current in order to prevent loss of efficiency from negative inductor.

PSYS

The PSYS pin is an analog input to the VR controller. It is a system input power monitor that facilitates the monitoring of the total platform system power. For more information regarding PSYS please contact Intel, Inc.

THEORY OF OPERATION

Input Voltage Feed−Forward (VRMP Pin)

Ramp generator circuits are provided for both the dual−edge modulator (only when it is operating in higher than 1 phase mode.) and two RPM modulators. The ramp generators implement input voltage feed−forward control by varying the ramp slopes proportional to the VRMP pin voltage. The VRMP pin also has a UVLO function, which is active only after the controller is enabled. The VRMP pin is high impedance input when the controller is disabled. For multi−phase operation, the dual−edge PWM ramp amplitude is changed according to the following:

$$VRMP\_pp = 0.1 \cdot Vvrmp \qquad \text{(eq. 2)}$$

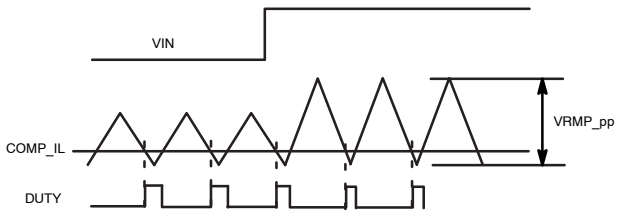


Figure 4. Ramp Feed Forward

Differential Current Feedback Amplifiers

Each phase of the two−phase rail has a low offset, differential amplifier to sense the current of that phase in order to balance current. The CSREF and CSPx pins are high impedance inputs, but it is recommended that any external filter resistor RCSN does not exceed 10 kΩ to avoid offset due to leakage current. It is also recommended that the voltage sense element be no less than 0.5 mΩ for best current balance.

The external filter RCSN and CCSN time constant should match the inductor L/DCR time constant, but fine tuning of this time constant is generally not required. Phase current signals are summed with the COMP or ramp signals at their respective PWM comparator inputs in order to balance phase currents via a current mode control approach.

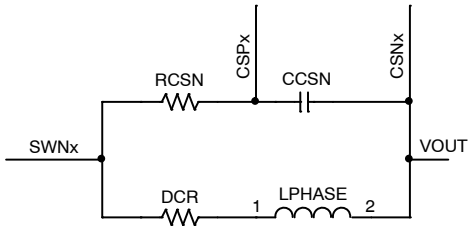


Figure 5. Per Phase Current Sense Network

$$R_{CSN} = \frac{L_{PHASE}}{C_{CSN} \cdot DCR} \qquad \text{(eq. 3)}$$

Total Current Sense Amplifier

The multiphase rail uses a patented approach to sum the phase currents into a single, temperature compensated, total current signal. This signal is then used to generate the output voltage droop, total current limit, and the output current monitoring functions. The Rref(n) resistors average the voltages at the output terminals of the inductors to create a low impedance reference voltage at CSREF. The Rph resistors sum currents from the switch nodes to the virtual CSREF potential created at the CSSUM pin by the amplifier.

The total current signal is the difference between the CSCOMP and CSREF voltages.

The amplifier filters, and amplifies, the voltage across the inductors in order to extract only the voltage across the inductor series resistances (DCR). An NTC thermistor (Rth) in the feedback network placed near the Phase 1 inductor senses the inductor temperature, and compensates both the DC gain and the filter time constant for the change in DCR with temperature. Phase 1 inductor is chosen for the thermistor location as this will be the only inductor in operation during single phase mode.

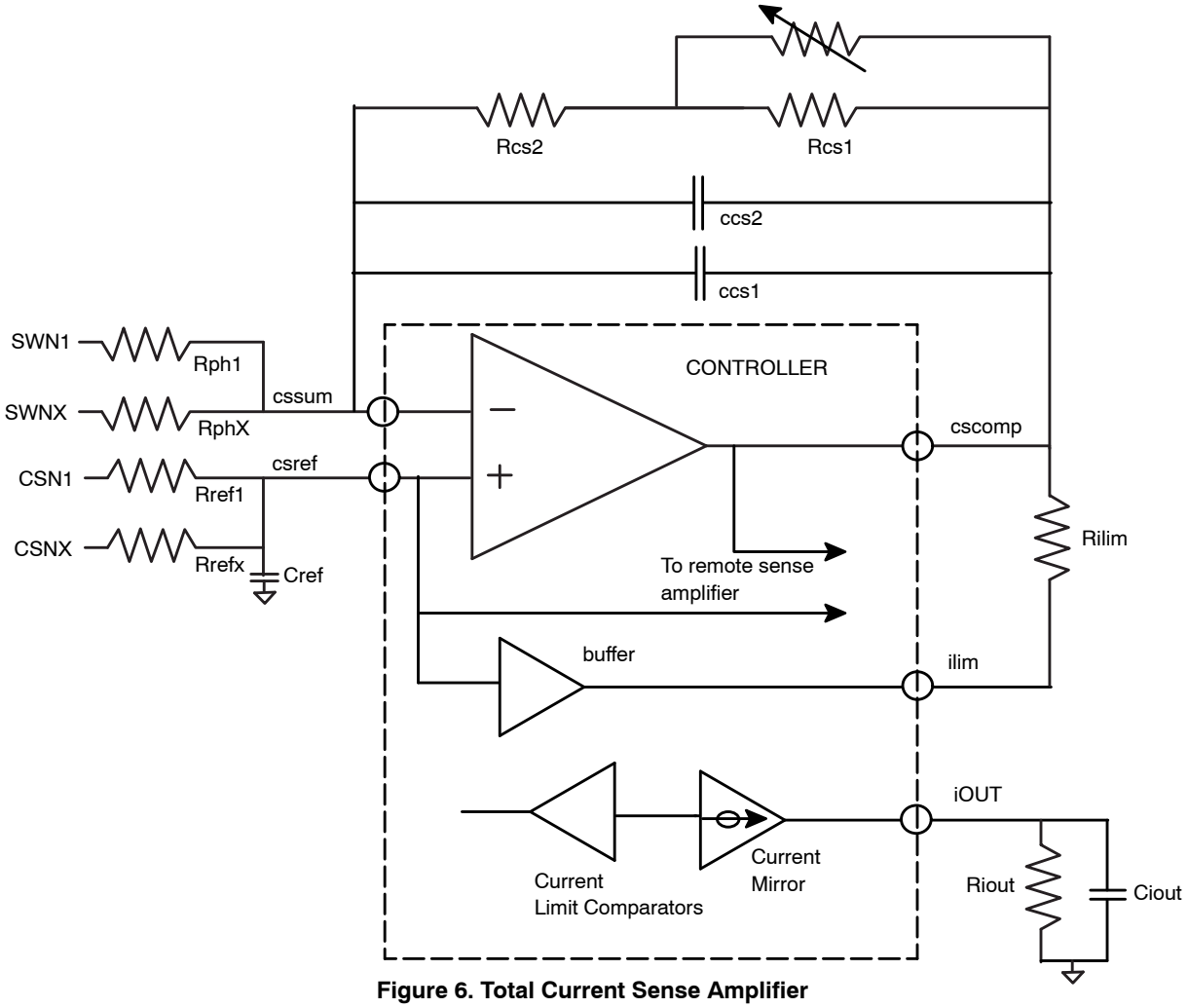


Figure 6. Total Current Sense Amplifier

The DC gain equation for the DC total current signal is:

$$V_{CSCOMP-CSREF} = \frac{Rcs2 + \frac{Rcs1 \cdot Rth}{Rcs1 + Rth}}{Rph} \cdot \left(Iout_{Total} \cdot DCR\right) \quad \text{(eq. 4)}$$

Set the DC gain by adjusting the value of the Rph resistors in order to make the ratio of total current signal to output current equal the desired loadline. The values of Rcs1 and Rcs2 are set based on the effect of temperature on both the thermistor and inductor, and may need to be adjusted to eliminate output voltage temperature drift with the final product enclosure and cooling.

The pole frequency of the CSCOMP filter should be set equal to the zero of the output inductor. This causes the total current signal to contain only the component of inductor voltage caused by the DCR voltage, and therefore to be proportional to inductor current. Connecting Ccs2 in parallel with Ccs1 allows fine tuning of the pole frequency using commonly available capacitor values. It is best to perform fine tuning during transient testing.

$$F_z = \frac{DCR@25°C}{2 \cdot \pi \cdot L_{phase}} \quad \text{(eq. 5)}$$

$$F_p = \frac{1}{2\pi \cdot \left(Rcs2 + \left(\frac{Rcs1 \cdot RTH}{Rcs1 + RTH}\right)\right) \cdot (CCs1 + CCs2)} \quad \text{(eq. 6)}$$

The value of the CREF capacitor (in nF) on the CSREF pin should be:

$$C_{cref} = \frac{0.02 \cdot RTH}{Rref} \quad \text{(eq. 7)}$$

Rail Remote Sense Amplifier

A high performance high input impedance true differential amplifier is provided to accurately sense regulator output voltage. The VSP and VSN inputs should be connected to the regulator's output voltage sense points. The remote sense amplifier takes the difference of the output voltage with the DAC voltage and adds the droop voltage.

$$V_{DIFOUT} = \left(V_{VSP} - V_{VSN}\right) + \left(1.3\ V - V_{DAC}\right) + \\ + \left(V_{DROOP} + V_{CSREF}\right) \quad \text{(eq. 8)}$$

This signal then goes through a standard error compensation network and into the inverting input of the error amplifier.

High Performance Voltage Error Amplifier

The Remote Sense Amplifier output feeds a Type III compensation network formed by the Error Amplifier and external tuning components. The non−inverting input of the error amplifier is connected to the same reference voltage used to bias the Remote Sense Amplifier output.

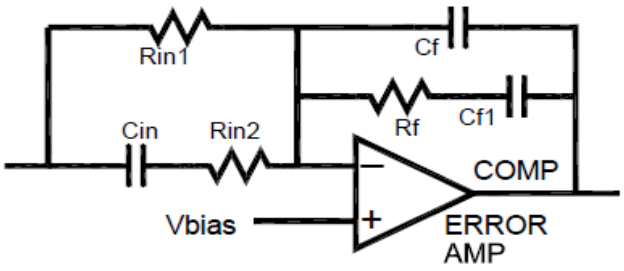


Figure 7. Error Amplifier

Loadline Programming (DROOP)

An output loadline is a power supply characteristic wherein the regulated (DC) output voltage decreases proportional to load current. This characteristic can reduce the output capacitance required to maintain output voltage within limits during load transients faster than those to which the regulation loop can respond.

A load line is produced by adding a signal proportional to output load current (VDROOP) to the output voltage feedback signal – thereby satisfying the voltage regulator at an output voltage reduced proportional to load current. The load line is programmed by setting the gain of the Total Current Sense Amplifier such that the total current signal is equal to the desired output voltage droop.

Programming the Current Limit

The current limit thresholds are programmed with a resistor between the ILIM and CSCOMP pins. The multiphase rails generates a replica of the CSREF pin voltage at the ILIM pin, and compares ILIM pin current to ICL and ICLM. The controller latches off if ILIM pin current exceeds ICL for t_OCPDLY, and latches off immediately if ILIM pin current exceeds ICLM. Set the value of the current limit resistor RLIMIT according to the desired current limit Iout LIMIT.

$$R_{LIMIT} = \frac{Rcs2 + \frac{Rcs1 \cdot Rth}{Rcs1 + Rth}}{Rph} \cdot \left(Iout_{LIMIT} \cdot DCR\right) \quad \text{(eq. 9)}$$
$$10\mu$$

Programming IOUT

The IOUT pin sources a current proportional to the ILIM current. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to ICCMAX generates a 2 V signal on IOUT. A pull−up resistor from 5 V VCC can be used to offset the IOUT signal positive if desired.

$$R_{Iout} = \frac{2.0\ V \cdot R_{LIMIT}}{10 \cdot \frac{Rcs2 + \frac{Rcs1 \cdot Rth}{Rcs1 + Rth}}{Rph} \cdot \left(Iout_{ICC\_MAX} \cdot DCR\right)} \quad \text{(eq. 10)}$$

Programming DAC Feed−Forward Filter

The multiphase rail outputs a pulse of current from the VSN pin upon each increment of the internal DAC following a dynamic voltage change up command. A parallel RC network inserted into the path from VSN to the output voltage return sense point, VSS_SENSE, causes these current pulses to temporarily decrease the voltage between VSP and VSN.

This causes the output voltage during dynamic voltage change to be regulated slightly higher, in order to compensate for the response of the Droop function to current flowing into the charging output capacitors. In the following equations, COUT is the total output capacitance of the system.

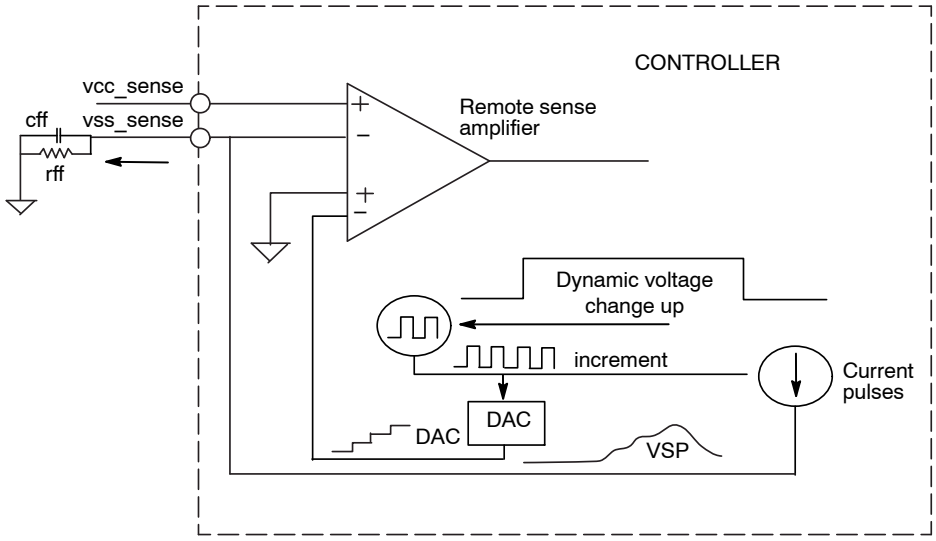


Figure 8. DAC Feed Forward

$$Rff = Cout \cdot Rout \cdot 453.6 \cdot 10^{6} \quad \text{(eq. 11)}$$

$$Cff = \frac{Rout \cdot Cout}{Rff} \quad \text{(eq. 12)}$$

Tsense Network

A temperature sense inputs is provided for the multiphase rail. A precision current is sourced out the output of the TSENSE pin to generate a voltage on the temperature sense networks. The voltages on the temperature sense inputs are sampled by the internal A/D converter. A 100k NTC similar to the Murata NCP15WF104E03RC should be used. Rcomp1 in the following Figure is optional, and can be used to slightly change the hysteresis. See the specification table for the thermal sensing voltage thresholds and source current.

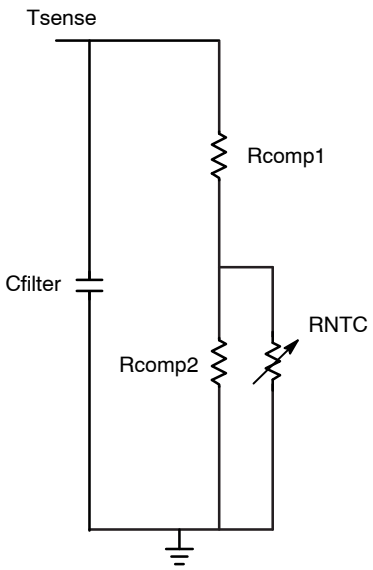


Figure 9. Tsense Network

PWM Comparators

The noninverting input of each comparator (one for each phase) is connected to the summation of the error amplifier output (COMP) and each phase current (IL*DCR*Phase Balance Gain Factor). The inverting input is connected to the triangle ramp voltage of that phase. The output of the comparator generates the PWM output.

During steady state operation, the main rail PWM pulses are centered on the valley of the triangle ramp waveforms and both edges of the PWM signals are modulated. During a transient event, the duty cycle can increase rapidly as the error amp signal increases with respect to the ramps, to provide a highly linear and proportional response to the step load.

Phase Detection Sequence

Normally, NCP81283 operates as a 6−phase PWM controller. During start−up, the number of operational phases and their phase relationship is determined by the internal circuitry monitoring the CSP outputs.

Table 3. PHASE DETECTION SEQUENCE

Configuration	Phase Configuration	Programming Pin CSPx	Unused Pins
1	6	All CSP pins connected normally	
2	5	Connect CSP6 to VCC through a 2k resistor. All other CSP pins connected normally	Float: PWM6, CSN6
3	4	Connect CSP5 to VCC through a 2k resistor pulled to VCC. All other CSP pins connected normally	Float: CSN5, CSN6, PWM5 and PWM6
4	3	Connect CSP4 through a 2k resistor pulled to VCC. All other CSP pins connected normally	Float: CSN4, CSN5, CSN6, PWM4, PWM5 and PWM6
5	2	Connect CSP3 through a 2k resistor pulled to VCC. All other CSP pins connected normally	Float: CSN3, CSN4, CSN5, CSN6, PWM3, PWM4, PWM5 and PWM6.
6	1	Connect CSP2 through a 2k resistor pulled to VCC. All other CSP pins connected normally	Float: CSN2, CSN3, CSN4, CSN5, CSN6, PWM3, PWM4, PWM5 and PWM6

*N is the phase configuration number in PS0.

Over Current Protection (OCP)

A programmable total current limit is provided that is decreased when not operating in PS0 mode. This limit is programmed with a resistor between the CSCOMP and ILIM pins. The current from the ILIM pin to this resistor is compared to the ILIM Threshold Currents.

If the fault is not removed, the controller shuts down when the timer expires. If the current into the pin exceeds ICLM, the controller shuts down immediately. To recover from an OCP fault, the EN pin or VCC voltage must be cycled low.

Input Under−Voltage Lockouts (UVLO)

The VR monitors the 5 V VCC supply as well as the VRMP pin voltage. Hysteresis is incorporated within these monitors.

Output Under Voltage Monitor

The multiphase phase rail output voltage is monitored for under voltage at the output of the differential amplifier. If the multiphase−phase rail output falls more than VUVM2 below the DAC−DROOP voltage, the UVM comparator will trip – sending the VR_RDY signal low.

Output Over Voltage Protection

The multiphase phase output voltage is monitored for OVP at the output of the differential amplifier and also at the CSREF pin. During normal operation, if an output voltage exceeds the DAC voltage by VOVP, the VR_RDY flag goes low, and the DAC voltage of the overvoltage rail will be slowly ramped down to 0 V to avoid producing a negative output voltage.

At the same time, the PWM outputs of the overvoltage rail are sent low. The PWM output will pulse to mid−level during the DAC ramp down period if the output decreases below the DAC + OVP Thsreshold as DAC decreases.

When the DAC gets to zero, the PWMs will be held low, and the VR will stay in this mode until the VCC voltage or EN is toggled.

Absolute OVP

During start up, the OVP threshold is set to the Absolute Over Voltage Threshold. This allows the controller to start up without false triggering OVP.

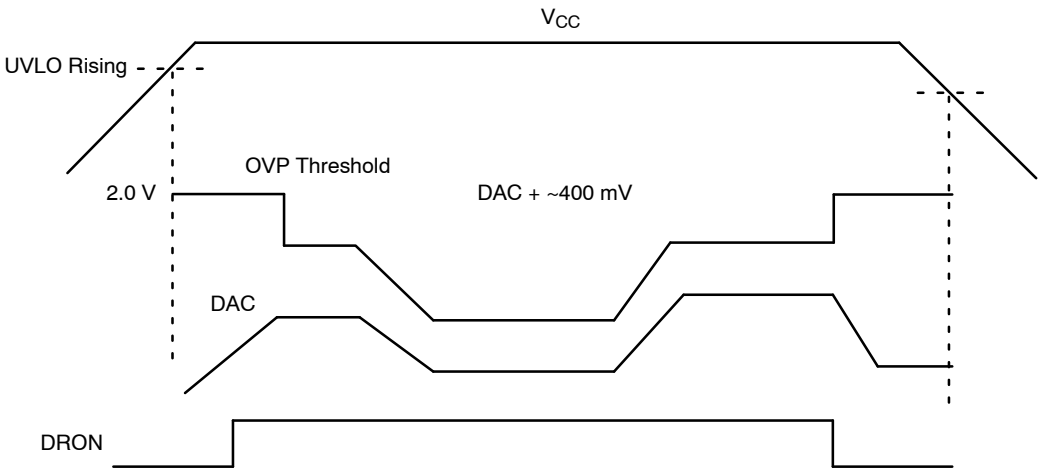


Figure 10. OVP Threshold Behavior

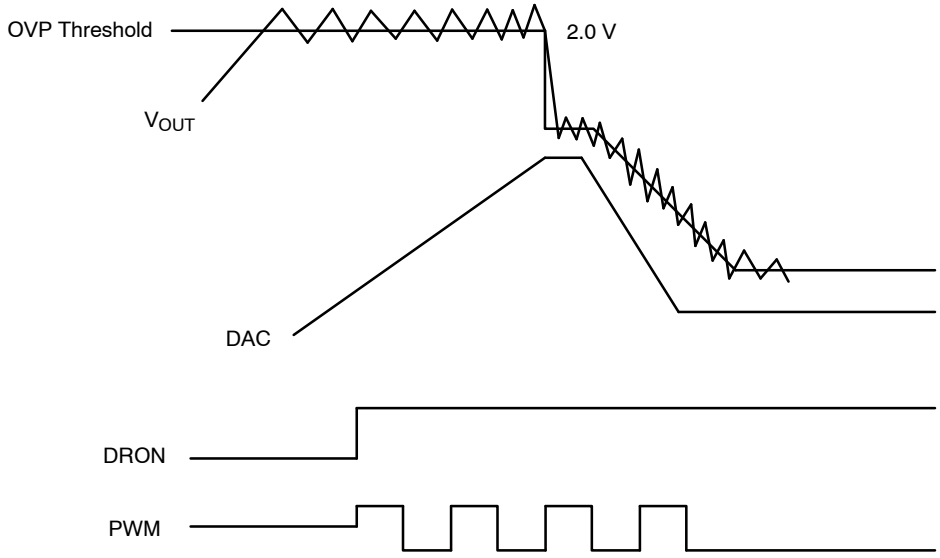


Figure 11. OVP Behavior at Start−up

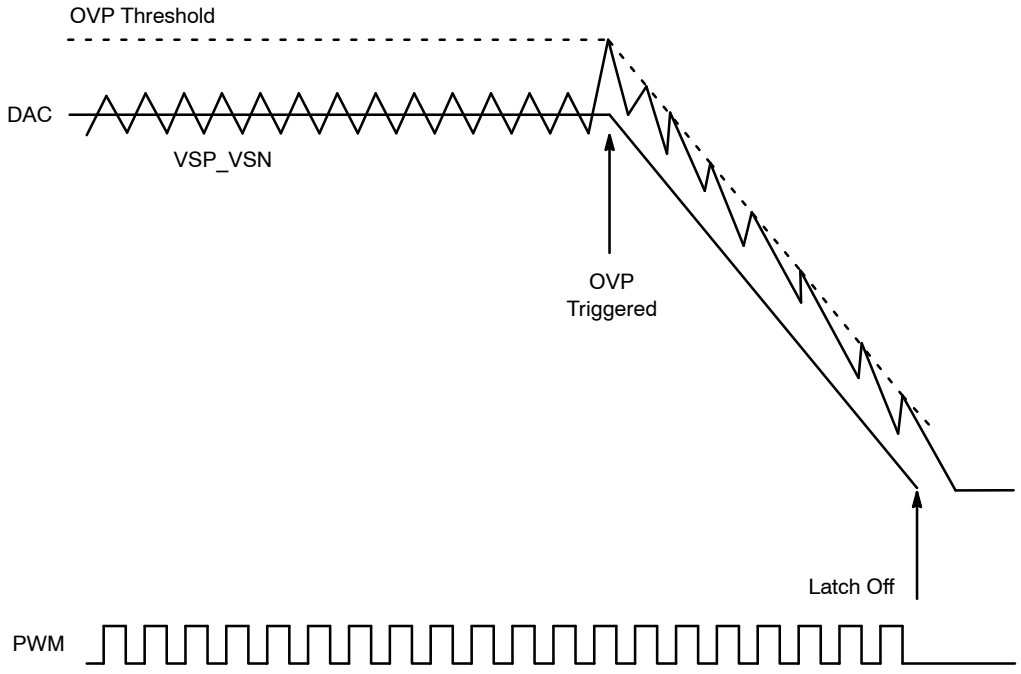


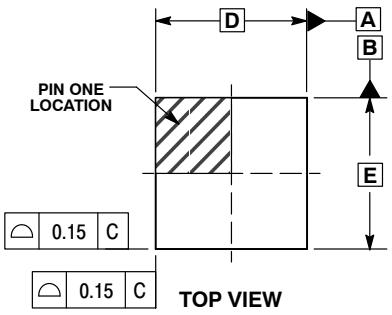
Figure 12. OVP during Normal Operation Mode

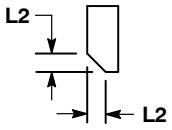
Serial VID Interface

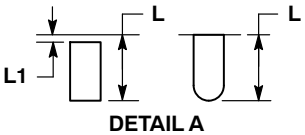
For Intel proprietary interface communication details please contact Intel, Inc.

PACKAGE DIMENSIONS

QFN40 5x5, 0.4P
CASE 485CR
ISSUE C

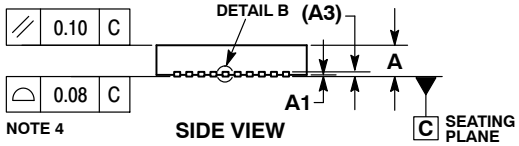


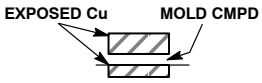




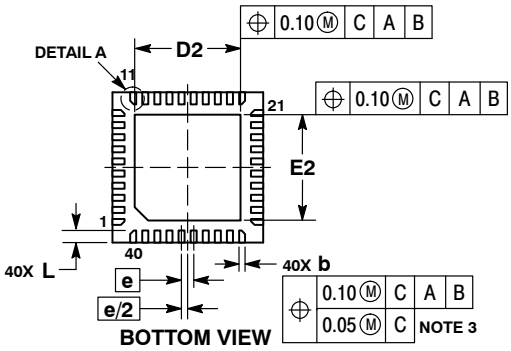
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.15	0.25
D	5.00 BSC	
D2	3.40	3.60
E	5.00 BSC	
E2	3.40	3.60
e	0.40 BSC	
L	0.30	0.50
L1	---	0.15
L2	0.12 REF	

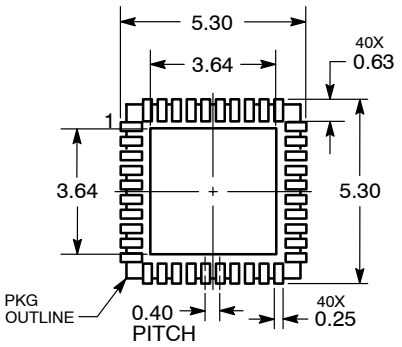




GENERIC MARKING DIAGRAM*



RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

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