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NTE74LS168A
NTE74LS169A
Integrated Circuit
TTL – Synchronous Presettable Up/Down Counter

Description:

The NTE74LS168A (BCD Decade) and NTE74LS169A (4–Bit Binary) are fully synchronous 4–stage up/down counters in a 16–Lead plastic DIP type package featuring a preset capability fo programmable operation, carry lookahead for easy cascading and an U/D input to control the direction of counting. The NTE74LS168A counts in a BCD decade (8, 4, 2, 1) sequence while the NTE74LS169A operates in a Modulo 16 binary sequence. All state changes, whether in counting or parallel loading, are initiated by the LOW–to–HIGH transition of the clock.

Features:

- Low Power Dissipation: 100mW (Typ)
- High–Speed Count Frequency: 30Mhz (Typ)
- Fully Synchronous Operation
- Full Carry Lookahead for Easy Cascading
- Single Up/Down Control Input
- Positive Edge–Trigger Operation
- Input Clamp Diodes Limit High–Speed Termination Effects

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
DC Input Voltage, V_{IN} 7V
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High–Level Output Current	I_{OH}	–	–	–0.4	mA
Low–Level Output Current	I_{OL}	–	–	8	mA
Operating Temperature Range	T_A	0	–	+70	°C

DC Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}			2	–	–	V
Low Level Input Voltage	V_{IL}			–	–	0.8	V
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −18mA		–	−0.65	−1.5	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX, I_{OH} = −400μA		2.7	3.5	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX	I_{OL} = 4mA	–	0.25	0.4	V
			I_{OL} = 8mA	–	0.35	0.5	V
Input Current	I_I	V_{CC} = MAX, V_I = 7V	$\overline{CET}$ Input	–	–	0.2	mA
			Other Inputs	–	–	0.1	mA
High Level Input Current	I_{IH}	V_{CC} = MAX, V_I = 2.7V	$\overline{CET}$ Input	–	–	40	μA
			Other Inputs	–	–	20	μA
Low Level Input Current	I_{IL}	V_{CC} = MAX, V_I = 0.4V	$\overline{CET}$ Input	–	–	−0.8	mA
			Other Inputs	–	–	−0.4	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 4		−20	–	−100	mA
Supply Current	I_{CC}	V_{CC} = MAX		–	–	34	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 4. Not more than one output should be shorted at a time and duration of short−circuit should not exceed one second.

AC Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	f_{max}	C_L = 15pF	25	32	–	MHz
Propagation Delay Time (From Clock Input to TC Output)	t_{PLH}		–	13	20	ns
	t_{PHL}		–	13	20	ns
Propagation Delay Time (From Clock Input to Any Q Output)	t_{PLH}		–	13	20	ns
	t_{PHL}		–	15	23	ns
Propagation Delay Time (From $\overline{CET}$ Input to TC Output)	t_{PLH}		–	15	20	ns
	t_{PHL}		–	15	20	ns
Propagation Delay Time (From U/D Input to TC Output)	t_{PLH}		–	17	25	ns
	t_{PHL}		–	19	29	ns

AC Setup Requirements: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Pulse Width	t_w		25	–	–	ns
Setup Time Data or Enable	t_{su}		20	–	–	ns
$\overline{PE}$			25	–	–	ns
U/D			30	–	–	ns
Hold Time, Any Input	t_h		0	–	–	ns

Functional Description:

The NTE74LS168A and NTE74LS169A use edge−triggering D−type flip−flops that have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a set−up time before the rising edge of the clock and remain valid for the recommended hold time thereafter.

The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is LOW, the data on the $P_0 - P_3$ inputs enters the flip−flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be LOW and $\overline{PE}$ must be HIGH. The U/$\overline{D}$ input then determines the direction of counting.

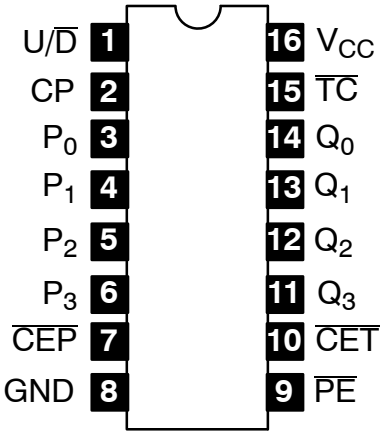
The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW, provided that $\overline{CET}$ is LOW, when a counter reaches zero in the COUNT DOWN mode or reaches 1 (9 for the NTE74LS168A) in the COUNT UP mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. The $\overline{TC}$ output of the NTE74LS168A decade counter can also be LOW in the illegal states 11, 13, and 15, which can occur when power is turned on via parallel loading. If illegal state occurs, the NTE74LS168A will return to the legitimate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip−flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended.

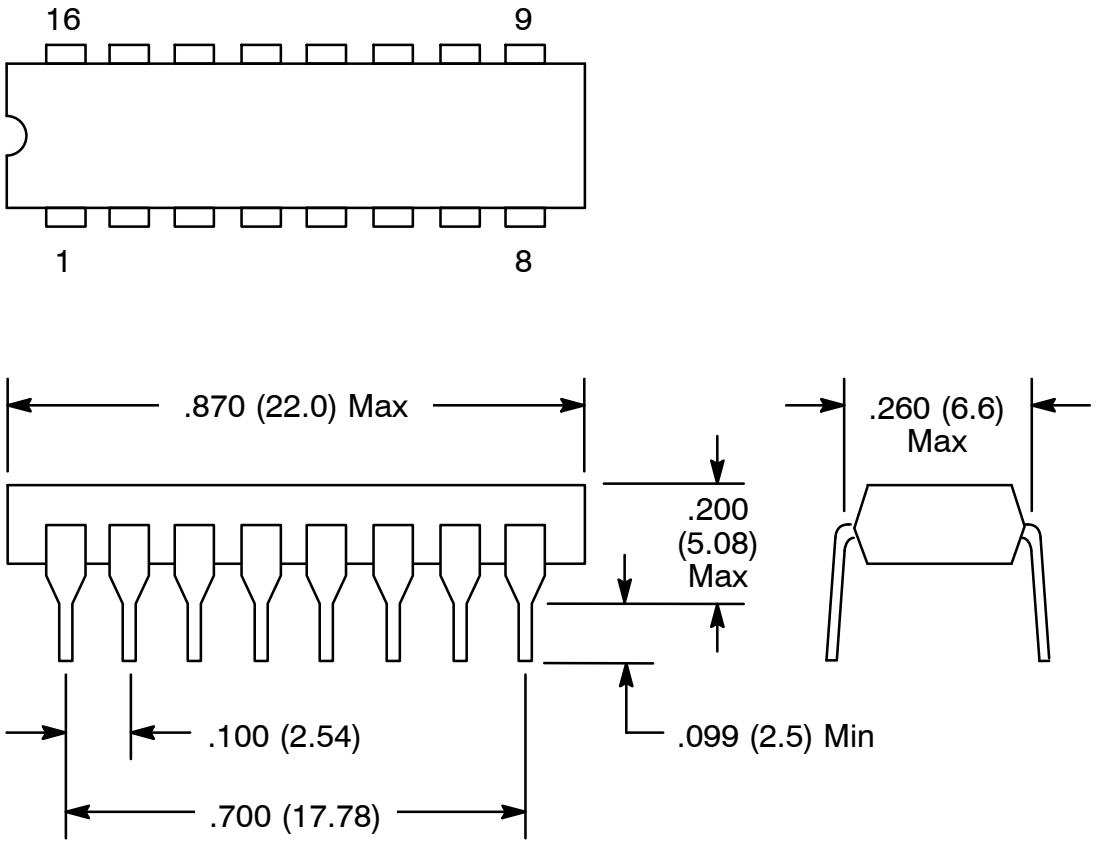
Mode Select Table:

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load (pn → Qn)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = HIGH Level
L = LOW Level
X = Immaterial

Pin Connection Diagram




16
9
1
8
.870 (22.0) Max
.260 (6.6)
Max
.200
(5.08)
Max
.100 (2.54)
.099 (2.5) Min
.700 (17.78)