ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE74H102
Integrated Circuit
TTL – AND–Gated J–K Negative–Edge–Triggered Flip–Flop with Preset and Clear

Description:

The NTE74H102 is a monolithic, J–K negative–edge–triggered flip–flop in a 14–Lead DIP type package that features gated J–K inputs and an asynchronous clear input. The AND gate inputs ae inhibited while he clock input is low; when the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum set–up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
DC Input Voltage, V_{IN} 5.5V
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High–Level Input Voltage	V_{IH}	2.0	–	–	V
Low–Level Input Voltage	V_{IL}	–	–	0.8	V
High–Level Output Current	I_{OH}	–	–	–0.5	μA
Low–Level Output Current	I_{OL}	–	–	20	mA
Pulse Duration CLK High	t_w	10	–	–	ns
CLK Low		15	–	–	ns
$\overline{CLR}$ or $\overline{PRE}$ Low		16	–	–	ns
Setup Time Before CLK ↓ High–Level Data	t_{su}	10	–	–	ns
Low–Level Data		13	–	–	ns
Hold Time After CLK ↓ High–Level Data	t_h	0	–	–	ns
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −8mA	–	–	−1.5	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −0.5mA	2.4	3.4	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 20mA	–	0.2	0.4	V
Input Current	I_I	V_{CC} = MAX, V_I = 5.5V	–	–	1	mA
High Level Input Current Any J or K	I_{IH}	V_{CC} = MAX, V_I = 2.4V	–	–	50	μA
$\overline{CLR}$			–	–	100	μA
$\overline{PRE}$			–	–	100	μA
CLK			0	–	−1	mA
Low Level Input Current Any J or K	I_{IL}	V_{CC} = MAX, V_I = 0.4V	–	−1	−2	mA
$\overline{CLR}$			–	−1	−2	mA
$\overline{PRE}$			–	−1	−2	mA
CLK			–	−3	−4.8	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 4	−40	–	−100	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 5	–	20	38	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 4. Not more than one output should be shorted at a time, and the duration of the short−circuit should not exceed one second.

Note 5. With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	f_{max}	R_L = 280Ω, C_L = 25pF	40	50	–	MHz
Propagation Delay Time (From $\overline{PRE}$ or $\overline{CLR}$ Input to Any Q Output)	t_{PLH}		–	8	12	ns
Propagation Delay Time (From $\overline{PRE}$ or $\overline{CLR}$ Input [CLK high] to Any Q Output)	t_{PLH}		–	15	20	ns
(From $\overline{PRE}$ or $\overline{CLR}$ Input [CLK low] to Any Q Output)			–	23	35	ns
Propagation Delay Time (From CLK Input to Any Q Output)	t_{PLH}		–	10	15	ns
	t_{PHL}		–	16	20	ns

Function Table:

Inputs					Outputs	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H †	H †
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Pin Connection Diagram