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NTE40160B, NTE40161B
NTE40162B, NTE40163B
Integrated Circuit
CMOS, Synchronous Programmable 4–Bit Counters

Description:

The NTE40160B (Decade w/Asynchronous Clear), NTE40161B (Binary w/Asynchronous Clear), NTE40162B (Decade w/Synchronous Clear), and NTE40163B (Binary w/Synchronous Clear) are 4–bit synchronous programmable counters in a 16–Lead DIP type package. The CLEAR function of the NTE40162B and NTE40163B is synchronous and a low level at the $\overline{\text{CLEAR}}$ input sets all four outputs low on the next positive CLOCK edge. The CLEAR function of the NTE40160B and NTE40161B is asynchronous and a low level at the $\overline{\text{CLEAR}}$ input sets all four outputs low regardless of the state of the CLOCK, $\overline{\text{LOAD}}$, or ENABLE inputs. A low level at the $\overline{\text{LOAD}}$ input disables the counter and causes the output to agree with the setup data after the next CLOCK pulse regardless of the conditions of the ENABLE inputs.

The carry look–ahead circuitry provides for cascading counters for n–bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count–enable inputs and a carry output (C_{OUT}). Counting is enabled when both PE and TE inputs are high. The TE input is fed forward to enable C_{OUT}. This enabled output produces a positive output pulse with a duration approximately equal to the positive portion of the Q1 output. This positive overflow carry pulse can be used to enable successive cascaded stages. Logic transitions at the PE or TE inputs may occur when the clock is either high or low.

Features:

- Internal Look–Ahead for Fast Counting
- Carry Output for Cascading
- Synchronous Programmable
- Clear Asynchronous Input: NTE40160B, NTE40161B
- Clear Synchronous Input: NTE40162B, NTE40163B
- Synchronous Load Control Input
- Low–Power TTL Compatibility
- Standardized, Symmetrical Output Characteristics
- Maximum Input Current of 1μA at 18V over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (over Full Package Temperature Range): 1V at V_{DD} = 5V, 2V at V_{DD} = 10V, 2.5V at V_{DD} = 15V
- 5V, 10V, and 15V Parametric Ratings

Applications:

- Programmable Binary and Decade Counting
- Counter Control/Timers
- Frequency Dividing

Absolute Maximum Ratings:

DC Supply Voltage Range (Voltages Referenced to V_{SS}), V_{DD} . . . . . −0.5 to +20V
Input Voltage Range (All Inputs) . . . . . −0.5 to V_{DD}+0.5V
DC Input Current (Any One Input) . . . . . ±10mA
Power Dissipation (Per Package), P_D
For T_A = −55° to +100°C 500mW
For T_A = +100° to +125°C . . . . . Derate Linearly at 12mW/°C to 200mW
Device Dissipation (Per Output Transistor)
For T_A = Full Package Temperature Range 100mW
Operating Temperature Range, T_A . . . . . −55° to +125°C
Storage Temperature Range, T_{stg} . . . . . −65° to +150°C
Lead Temperature (During Soldering, 10sec), T_L . . . . . +265°C

Recommended Operating Conditions: (T_A = +25°C, Note 1 unless otherwise specified)

Parameter	Symbol	V_{DD} (V)	Limits		Unit
			Min	Max	
Supply Voltage Range (Full T_A = Full Package Temperature Range)	–	–	3	18	V
Setup Time	t_{SU}				
Data to Clock		5	240	–	
		10	90	–	
		15	60	–	
$\overline{\text{Load}}$ to Clock		5	240	–	ns
		10	90	–	ns
		15	60	–	ns
PE o TE to Clock		5	340	–	ns
		10	140	–	ns
		15	100	–	ns
$\overline{\text{Clear}}$ to Clock (NTE40162B, NTE40163B **ONLY**)		5	340	–	ns
		10	140	–	ns
		15	100	–	ns
All Hold Times	t_H	5	0	–	ns
		10	0	–	ns
		15	0	–	ns
$\overline{\text{Clear}}$ Removal Time (NTE40160B, NTE40161B **ONLY**)	t_{rem}	5	200	–	ns
		10	100	–	ns
		15	70	–	ns
$\overline{\text{Clear}}$ Pulse Width (NTE40160B, NTE40161B **ONLY**)	t_{WL}	5	170	–	ns
		10	70	–	ns
		15	50	–	ns
Clock Input Frequency	f_{CL}	5	–	2.0	Mhz
		10	–	5.5	Mhz
		15	–	8.0	MHz
Clock Pulse Width	t_W	5	170	–	ns
		10	70	–	ns
		15	50	–	ns
Clock Rise or Fall Time	t_rCL	5	–	200	µs
	t_fCL	10	–	70	µs
		15	–	15	µs

Note 1. For maximum reliability, nominal operating conditions should be selected so that operation is always within the above ranges.

Static Electrical Characteristics:

Characteristic	Conditions			Limits at Indicated Temperature (°C)							Units
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55°C	–40°C	+85°C	+125°C	+25°C			
								Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max	–	0,5	5	5	5	150	150	–	0.04	5	µA
	–	0,10	10	10	10	300	300	–	0.04	10	µA
	–	0,15	15	20	20	600	600	–	0.04	20	µA
	–	0,20	20	100	100	3000	3000	–	0.08	1000	µA
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1.0	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	mA
	1.5	0,15	15	4.2	4.0	2.8	2.4	3.4	6.8	–	mA
Output High (Source) Current I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1.0	–	mA
	2.5	0.5	5	–2.0	–1.8	–1.3	–1.15	–1.6	–3.2	–	mA
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	mA
	13.5	0,15	15	–4.2	–4.0	–2.8	–2.4	–3.4	–6.8	–	mA
Output Voltage Low–Level V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	V
	–	0,15	15	0.05				–	0	0.05	V
Output Voltage High–Level V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	V
	–	0,10	10	9.95				9.95	10	–	V
	–	0,15	15	14.95				14.95	15	–	V
Input Voltage Low–Level V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3.0				–	–	3.0	V
	1.5,13.5	–	15	4.0				–	–	4.0	V
Input Voltage High–Level V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	V
	1.9	–	10	7.0				7.0	–	–	V
	1.5,13.5	–	15	11.0				11.0	–	–	V
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1.0	±1.0	–	$\pm10^{-5}$	±0.1	µA

Dynamic Electrical Characteristics:

(T_A = +25°C, C_L = 50pF, R_L = 200kΩ, t_r and t_f = 20ns unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Operation						
Propagation Delay Time Clock to Q	t_{PHL} or t_{PLH}	V_{DD} = 5V	–	200	400	ns
		V_{DD} = 10V	–	80	160	ns
		V_{DD} = 15V	–	60	120	ns
Clock to C_{OUT}		V_{DD} = 5V	–	225	450	ns
		V_{DD} = 10V	–	95	190	ns
		V_{DD} = 15V	–	70	140	ns
TE to C_{OUT}		V_{DD} = 5V	–	126	250	ns
		V_{DD} = 10V	–	55	110	ns
		V_{DD} = 15V	–	40	80	ns

Dynamic Electrical Characteristics (Cont'd): (T_A = +25°C, C_L = 50pF, R_L = 200kΩ, t_r and t_f = 20ns unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Minimum Setup Time Data to Clock	t_{SU}	V_{DD} = 5V	–	120	240	ns
		V_{DD} = 10V	–	45	90	ns
		V_{DD} = 15V	–	30	60	ns
$\overline{\text{Load}}$ to Clock		V_{DD} = 5V	–	120	240	ns
		V_{DD} = 10V	–	45	90	ns
		V_{DD} = 15V	–	30	60	ns
PE to TE to Clock		V_{DD} = 5V	–	170	340	ns
		V_{DD} = 10V	–	70	140	ns
		V_{DD} = 15V	–	50	100	ns
Minimum Hold Time	t_H	V_{DD} = 5V	–	–	0	ns
		V_{DD} = 10V	–	–	0	ns
		V_{DD} = 15V	–	–	0	ns
Transition Time	t_{THL}, t_{TLH}	V_{DD} = 5V	–	100	200	ns
		V_{DD} = 10V	–	50	100	ns
		V_{DD} = 15V	–	40	80	ns
Minimum Clock Pulse Width	t_W	V_{DD} = 5V	–	85	170	ns
		V_{DD} = 10V	–	35	70	ns
		V_{DD} = 15V	–	25	50	ns
Maximum Clock Frequency	f_{CL}	V_{DD} = 5V	2.0	3.0	–	MHz
		V_{DD} = 10V	5.5	8.5	–	MHz
		V_{DD} = 15V	8.0	12.0	–	MHz
Maximum Clock Rise or Fall Time (Note 2)	$t_{Wr}CL$, t_fCL	V_{DD} = 5V	200	–	–	µs
		V_{DD} = 10V	70	–	–	µs
		V_{DD} = 15V	15	–	–	µs
Clear Operation						
Propagation Delay Time NTE40160B, NTE40161B **ONLY** $\overline{\text{Clear}}$ to Q	t_{PHL}	V_{DD} = 5V	–	250	500	ns
		V_{DD} = 10V	–	110	220	ns
		V_{DD} = 15V	–	80	160	ns
Minimum Setup Time NTE40162B, NTE40163B **ONLY** $\overline{\text{Clear}}$ to Clock	t_{SU}	V_{DD} = 5V	–	170	340	ns
		V_{DD} = 10V	–	70	140	ns
		V_{DD} = 15V	–	50	100	ns
Minimum Hold Time NTE40162B, NTE40163B **ONLY** $\overline{\text{Clear}}$ to Clock	t_H	V_{DD} = 5V	–	–	0	ns
		V_{DD} = 10V	–	–	0	ns
		V_{DD} = 15V	–	–	0	ns

Note 2. If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the fixed propagation delay at 50pF and the transition time of the carry output driving stage for the estimated capacitive load.

Dynamic Electrical Characteristics (Cont'd): (T_A = +25°C, C_L = 50pF, R_L = 200kΩ, t_r and t_f = 20ns unless otherwise specified)

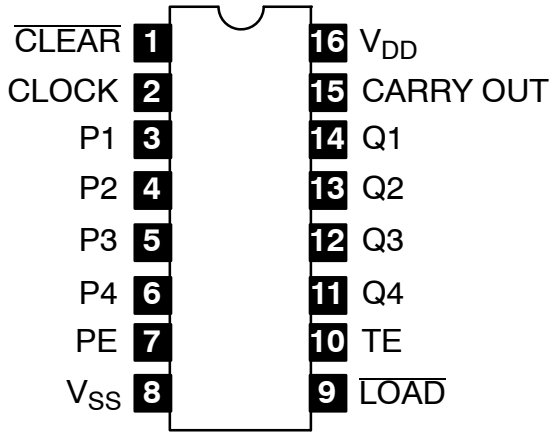
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Minimum $\overline{\text{Clear}}$ Removal Time NTE40160B, NTE40161B **ONLY**	t_{rem}	V_{DD} = 5V	–	100	200	ns
		V_{DD} = 10V	–	50	100	ns
		V_{DD} = 15V	–	35	70	ns
Minimum $\overline{\text{Clear}}$ Pulse Width NTE40160B, NTE40161B **ONLY**	t_{WL}	V_{DD} = 5V	–	85	170	ns
		V_{DD} = 10V	–	35	70	ns
		V_{DD} = 15V	–	25	50	ns

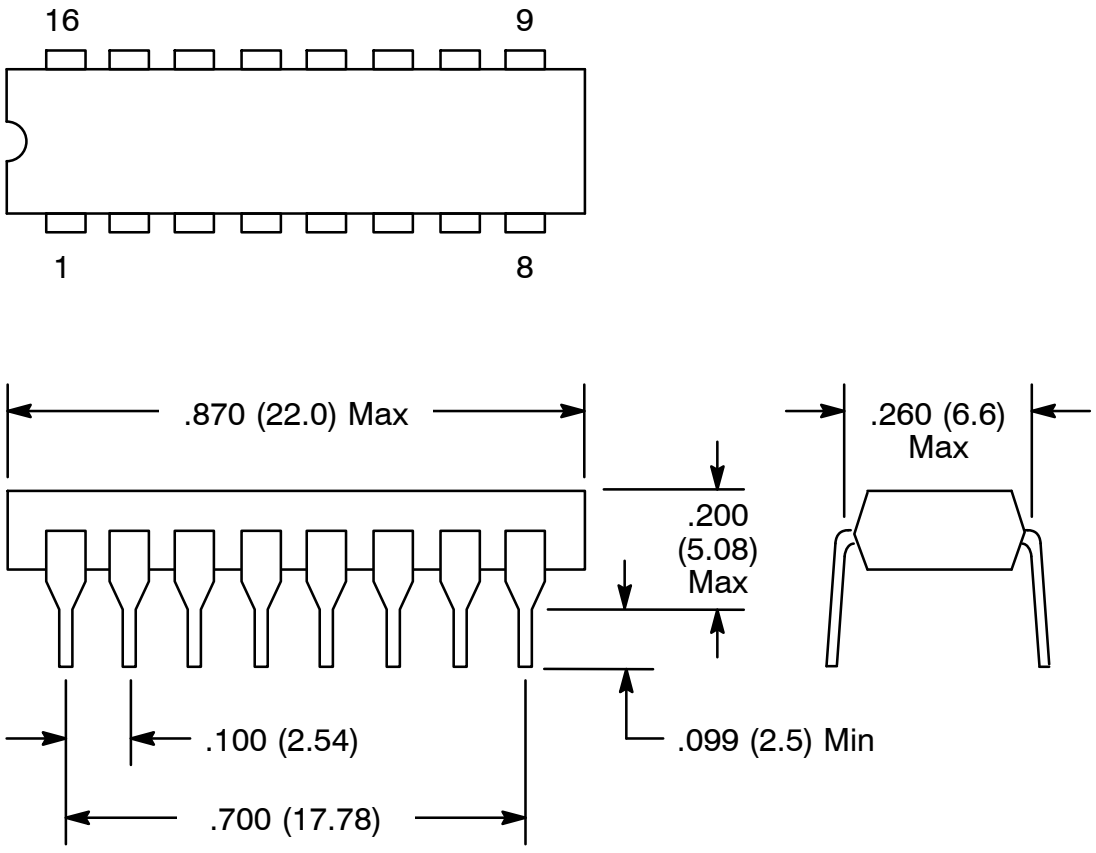
Truth Table

CLOCK	$\overline{\text{CLR}}$	$\overline{\text{LOAD}}$	PE	TE	Operation
⎍	1	0	X	X	PRESET
⎍	1	1	0	X	NC
⎍	1	1	X	0	NC
⎍	1	1	1	1	COUNT
X	0	X	X	X	RESET **(NTE40160B, NTE40161B)**
⎍	0	X	X	X	RESET **(NTE40162B, NTE40163B)**
⎎	1	X	X	X	NC **(NTE40162B, NTE40163B)**

1 = High Level
0 = Low Level
X = Don't Care
NC = No Change

Pin Connection Diagram




16
9
1
8
.870 (22.0) Max
.260 (6.6)
Max
.200
(5.08)
Max
.100 (2.54)
.099 (2.5) Min
.700 (17.78)