F-RAM Technology Brief

Overview

Established semiconductor memory technologies are divided into two categories:

1. RAMs are Random Access Memories, which simply means that the access time for reads and writes are symmetric.

2. Nonvolatile memories have traditionally been ROM (Read Only Memory) until the advent of floating gate technology, which produced electrically erasable memories such as Flash and EEPROM. These products allow for in-system programming but read and write access times are dissimilar. In fact, the write access times can be several orders of magnitude greater than the read access times.

Ferroelectric Random Access Memory or F-RAM has attributes that make it the ideal nonvolatile memory. It is a true nonvolatile RAM. The write advantages and non-volatility make it quite suitable for storing data in the absence of power.

Ferroelectric Property

The ferroelectric property is a phenomena observed in a class of materials known as Perovskites. Figure 1 shows a Perovskite crystal. The atom in the center has two equal and stable low energy states. These states determine the position of the atom. If a field is applied in the proper plane, the atom will move in the direction of the field.

Applying an electric field across the crystal causes the low energy state or position to be in the direction of the field and, conversely, the high energy state in the opposite position. The applied field will, therefore, cause the atom to move from the high energy state to the low energy state. This transition produces energy in the form of charge generally referred to as switch charge (Qs). Therefore, applying an alternating electric field across the crystal will cause the atom to move from the top of the crystal to the bottom and back again. Each transition will produce charge, Qs.

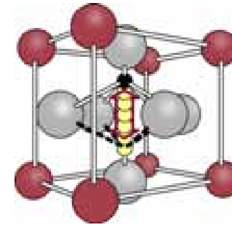

Figure 1. Ferroelectric (Perovskite) Crystal

A common misconception is that ferroelectric crystals are ferromagnetic or have similar properties. The term "ferroelectric" refers to similarity of the graph of charge plotted as a function of voltage (Figure 2) to the hysteresis loop (BH curve) of ferromagnetic materials. **Ferroelectric materials switch in an electric field and are not affected by magnetic fields.**

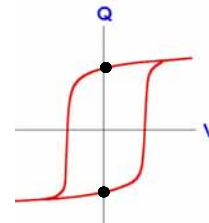

Figure 2. Ferroelectric Hysteresis Loop

The ferroelectric material has two states, the atom at the top, which is referred to as up polarization, and the atom at the bottom, which is referred to as down polarization (Figure 3). Therefore, with a viable sensing scheme a binary memory can be produced.

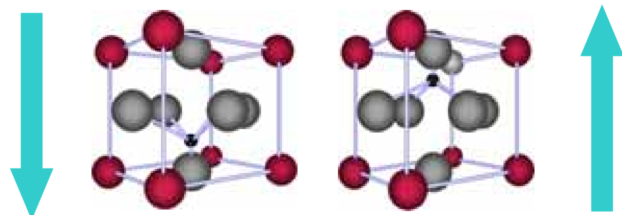

Figure 3. Crystal Polarization

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F-RAM Operation

The basic storage element is a ferroelectric capacitor. The capacitor can be polarized up or down by applying a field (Figure 4).

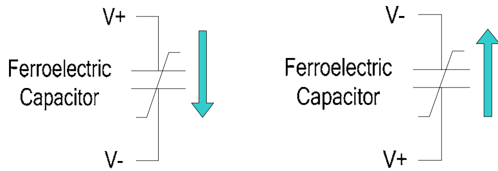

Figure 4. Ferroelectric Capacitor Polarization

The ferroelectric capacitor symbol indicates that the capacitance is variable and is not a traditional linear capacitor. If a ferroelectric capacitor is not switched when an electric field is applied (no change in polarization), it behaves like a linear capacitor. If it is switched, there is an additional charge induced, hence the capacitance must increase.

The ferroelectric capacitor is combined with an access transistor, a bit line, and a plate line to form the memory cell (Figure 5).

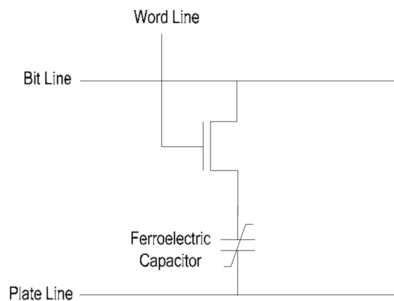

Figure 5. F-RAM Memory Cell

Read Operation

The static state of the cell is Bit Line low, Plate Line low, Word Line low (Figure 6A). The access begins by applying voltage to the Word Line and the Plate Line (6B). This applies a field across the ferroelectric capacitor and the ferroelectric capacitor switches (6C). The induced charge (Qs) is shared with the parasitic Bit Line capacitance (Cbit) and the switched ferroelectric capacitor (Cs). The voltage on the bit line, therefore, is proportional to the ratio of the capacitances Cs/Cbit (Cs includes a small contribution from transistor and interconnect parasitics).

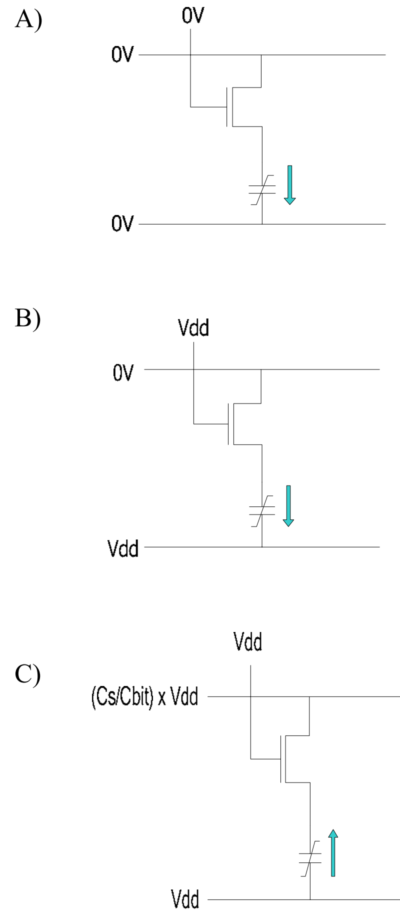

Figure 6. Memory Cell Access Sequence

Figure 6 shows the switched case. Had the polarization been up in this sequence, the capacitor would not switch and there would be no additional charge induced. The charge induced in the switched capacitor is at least two times greater than the charge available in the unswitched capacitor (Qu).

$$Qs \geq 2Qu$$

Therefore, the switched capacitance (Cs) is at least twice the unswitched capacitance (Cu).

$$Cs \geq 2Cu$$

It follows that the Bit Line voltage for the switched case is at least two times greater then the Bit Line voltage for the unswitched case.

The sensing scheme is very similar to the techniques used in DRAMs. The Bit Line voltage is simply compared to a reference that is above the unswitched value and below the switched value. The sense amp drives the Bit Lines to the rails and the output of the

sense amp is either high or low (1 or 0). The access is completed in less than 100ns.

At the end of the access the Bit Lines are set high for the switched case and set low for the unswitched case. The cycle is completed by bringing the Plate Line low, which restores the state of the switched terms and then the Bit Line is precharged to 0V. The restore/precharge period is also very fast, less than 100ns. The minimum achievable access/cycle times are primarily driven by the capacitance of the memory cell. The time it takes to switch the ferroelectric capacitor is nearly instantaneous and, therefore, switching mechanisms does not contribute to the overall cycle time.

The sensing scheme is similar to DRAMs because both F-RAM and DRAM sense charge. The charge in a DRAM is stored in a linear capacitor that leaks and requires refresh. The charge in an F-RAM is stored as state in the crystal and is, therefore, nonvolatile and requires no refresh. Like DRAMs, F-RAMs have a cycle time, so the minimum time between back-to-back random addresses is equal to the cycle time, not the access time. Today, typical cycle times are less than 200ns and in the near future should be less the 100ns.

Write Operation

A write operation is very similar to a read operation. The circuit simply applies a field in the desired direction across the ferroelectric capacitor.

F-RAM Milestones

1984	Ramtron founded to develop F-RAM technology
1989	First F-RAM fab installed for process development
1993	First F-RAM commercial product introduced
	4Kbit F-RAM memory in volume production
1996	16Kbit F-RAM memory in volume production
1998	Mass production of F-RAM at 1.0µ
1999	Mass production of 0.5µ F-RAM
	64Kbit, 256Kbit F-RAM memories in production
2000	3V operation F-RAM products demonstrated
2001	3V operation products enter production
2001	0.35µ process enters production
2002	256Kbit w/Real Time Clock
2004	Ramtron F-RAM shipments cross 50 million units
2005	First 1Mbit F-RAM sample
2006	Ramtron F-RAM shipments cross 150 million units
2006	First AEC-Q100 Qualified F-RAM
2007	First 0.13µ 4Mbit F-RAM
2007	First F-RAM-enhanced 8051 MCU

F-RAM Benefits

Traditional writable nonvolatile memories derived from floating gate technology use charge pumps to develop high voltage on-chip (10V or more) to force carriers through the gate oxide. Therefore, there are long write delays, high write power, and the write operation is actually destructive to the memory cell.

Floating gate devices are incapable of supporting writes that exceed 10^6 accesses. To put this in perspective, a data recorder using EEPROM that was recording data at 1 sample/s would wear out in less than 12 days. In comparison, the 3V F-RAM products offer virtually unlimited endurance (10^{15} accesses).

The F-RAM is far superior to floating gate devices in both write speed and power. For a typical serial EEPROM with a clock rate of 20MHz, it will take 5ms to write 32 bytes (page buffer). For an equivalent F-RAM, it will take 2ms to write 4K bytes. In addition, it requires 10.5mJ to write 4K bytes for the EEPROM versus 27µJ to write 4K bytes to an F-RAM.

In summary:

- **Read Access Time = Write Access Time <100ns**
- **Read Energy = Write Energy**
- **High Write Endurance**

Applications

1. Power failure

Any nonvolatile memory can retain a configuration. However, if the configuration changes and power failure is a possibility, the higher write endurance of F-RAM allows changes to be recorded without restriction. Any time the system state changes, it writes the new state. This avoids writing to memory on power down when the available time is short and power is disappearing.

2. RF/ID

In the area of contactless memory, F-RAM provides an ideal solution. Since RF/ID memory is powered by an RF field, and the available energy in the field declines exponentially with distance, low energy access is critical. The tag must be close enough to the field to induce the minimum amount of energy to write and it must extract the energy while in the field. Applications that require writes (e.g. debit cards, tags used in manufacturing processes) benefit from improved write distance, lower sensitivity to motion (time in the field), and lower RF power required for the transmitter /receiver.

3. High noise environments

Writing to EEPROM in a noisy environment can be challenging. When severe noise or power fluctuations are present, the long write time of EEPROM creates a window of vulnerability (measured in milliseconds) during which the write can be corrupted. The probability of errors is proportional to the size of the window. A write transaction window for F-RAM is less than 200ns.

4. Diagnostic/Maintenance

In a sophisticated system, the operating history and system state during a failure is important knowledge. Troubleshooting or maintenance is expedited when this information has been recorded. Due to the high write endurance, F-RAM makes an ideal system log. Diverse systems from workstations to industrial process control can benefit from this approach.