



## N-Channel Depletion-Mode Vertical DMOS FET

### Features

- ▶ High input impedance
- ▶ Low input capacitance
- ▶ Fast switching speeds
- ▶ Low on-resistance
- ▶ Free from secondary breakdown
- ▶ Low input and output leakage

### Applications

- ▶ Normally-on switches
- ▶ Solid state relays
- ▶ Converters
- ▶ Linear amplifiers
- ▶ Constant current sources
- ▶ Battery operated systems
- ▶ Telecom

### General Description

The DN2470 is a low threshold depletion-mode (normally-on) transistor utilizing an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FET is ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Ordering Information

Device	Package	$BV_{DSX}/BV_{DGX}$ (V)	$R_{DS(ON)}$ (max) ( $\Omega$ )	$I_{DSS}$ (typ) (mA)
	TO-252 (D-PAK)			
DN2470	DN2470K4-G	700	42	500

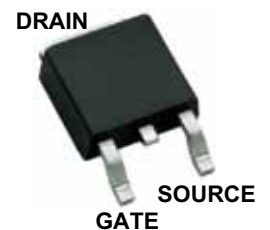


### Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	$BV_{DSX}$
Drain-to-gate voltage	$BV_{DGX}$
Gate-to-source voltage	$\pm 20V$
Operating and storage temperature	$-55^{\circ}C$ to $+150^{\circ}C$

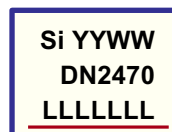
*Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.*

### Package



**TO-252 (D-PAK) (K4)**

### Product Marking



YY = Year Sealed  
WW = Week Sealed  
L = Lot Number  
\_\_\_\_\_ = "Green" Packaging

Package may or may not include the following marks: Si or

**TO-252 (D-PAK) (K4)**

## Thermal Characteristics

Package	$I_D$ (continuous) <sup>†</sup> (mA)	$I_D$ (pulsed) (mA)	Power Dissipation @ $T_A = 25^\circ\text{C}$ (W)	$\theta_{jc}$ ( $^\circ\text{C}/\text{W}$ )	$\theta_{ja}$ ( $^\circ\text{C}/\text{W}$ )	$I_{DR}^{\dagger}$ (mA)	$I_{DRM}$ (mA)
TO-252	170	500	2.5 <sup>‡</sup>	6.25	50 <sup>‡</sup>	170	500

### Notes:

<sup>†</sup>  $I_D$  (continuous) is limited by max rated  $T_J$  of  $150^\circ\text{C}$ .

<sup>‡</sup> Mounted on FR4 board, 25mm x 25mm x 1.57mm

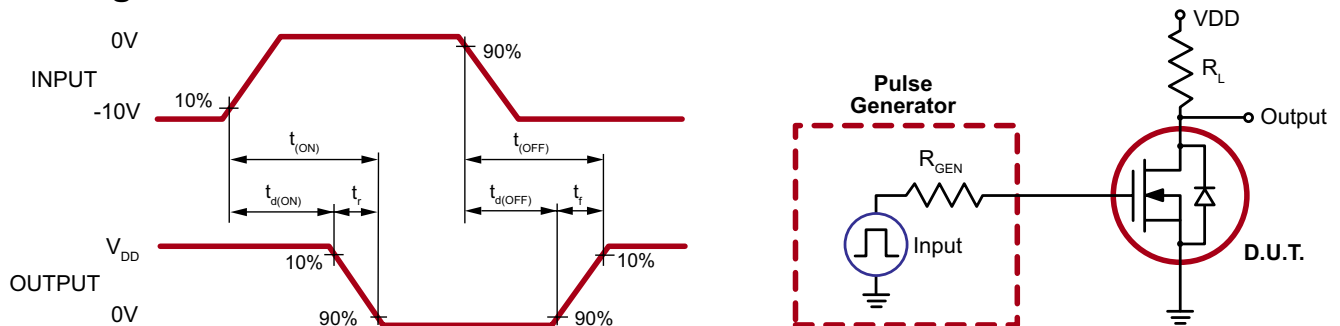
## Electrical Characteristics ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$BV_{DSX}$	Drain-to-source breakdown voltage	700	-	-	V	$V_{GS} = -5.0\text{V}$ , $I_D = 100\mu\text{A}$
$V_{GS(OFF)}$	Gate-to-source off voltage	-1.5	-	-3.5	V	$V_{DS} = 25\text{V}$ , $I_D = 10\mu\text{A}$
$\Delta V_{GS(OFF)}$	Change in $V_{GS(OFF)}$ with temperature	-	-	-4.5	mV/ $^\circ\text{C}$	$V_{DS} = 25\text{V}$ , $I_D = 10\mu\text{A}$
$I_{GSS}$	Gate body leakage current	-	-	100	nA	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$
$I_{D(OFF)}$	Drain-to-source leakage current	-	-	1.0	$\mu\text{A}$	$V_{GS} = -10\text{V}$ , $V_{DS} = \text{Max rating}$
		-	-	1.0	mA	$V_{GS} = -10\text{V}$ , $T_A = 125^\circ\text{C}$ , $V_{DS} = 0.8 \text{ Max Rating}$
$I_{DSS}$	Saturated drain-to-source current	-	500	-	mA	$V_{GS} = 0\text{V}$ , $V_{DS} = 25\text{V}$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	-	42	$\Omega$	$V_{GS} = 0\text{V}$ , $I_D = 100\text{mA}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.1	%/ $^\circ\text{C}$	$V_{GS} = 0\text{V}$ , $I_D = 100\text{mA}$
$G_{FS}$	Forward transconductance	100	-	-	mmho	$V_{DS} = 10\text{V}$ , $I_D = 100\text{mA}$
$C_{ISS}$	Input capacitance	-	-	540	pF	$V_{GS} = -10\text{V}$ , $V_{DS} = 25\text{V}$ , $f = 1.0\text{MHz}$
$C_{OSS}$	Common source output capacitance	-	-	60		
$C_{RSS}$	Reverse transfer capacitance	-	-	25		
$t_{d(ON)}$	Turn-on delay time	-	-	30	ns	$V_{DD} = 25\text{V}$ , $I_D = 100\text{mA}$ , $R_{GEN} = 25\Omega$
$t_r$	Rise time	-	-	45		
$t_{d(OFF)}$	Turn-off delay time	-	-	45		
$t_f$	Fall time	-	-	60		
$V_{SD}$	Diode forward voltage drop	-	-	1.8	V	$V_{GS} = -5.0\text{V}$ , $I_{SD} = 200\text{mA}$
$t_{rr}$	Reverse recovery time	-	800	-	ns	$V_{GS} = -5.0\text{V}$ , $I_{SD} = 200\text{mA}$

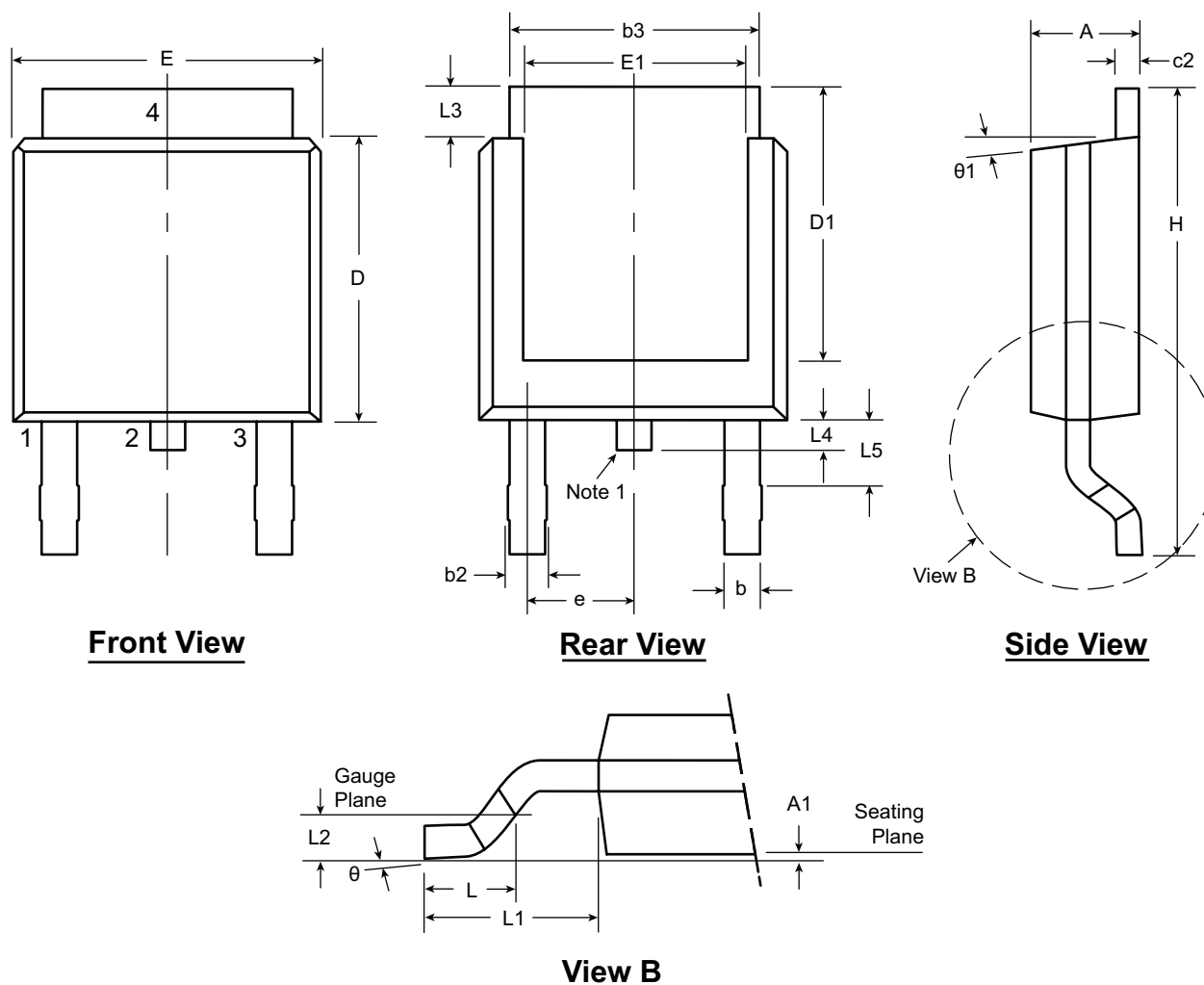
### Notes:

1. All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test: 300 $\mu\text{s}$  pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

## Switching Waveforms and Test Circuit



## 3-Lead TO-252 (D-PAK) Package Outline (K4)



**Note:**

1. Although 4 terminal locations are shown, only 3 are functional. Lead number 2 was removed.

Symbol		A	A1	b	b2	b3	c2	D	D1	E	E1	e	H	L	L1	L2	L3	L4	L5	θ	θ1
Dimension (inches)	MIN	.086	.000*	.025	.030	.195	.018	.235	.205	.250	.170	.090 BSC	.370	.055	.108 REF	.020 BSC	.035	.025*	.035†	0°	0°
	NOM	-	-	-	-	-	-	.240	-	-	-		.060	-			-	-	-	-	
	MAX	.094	.005	.035	.045	.215	.035	.245	.217*	.265	.200*		.410	.070			.050	.040	.060	10°	15°

JEDEC Registration TO-252, Variation AA, Issue E, June 2004.

\* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

**Drawings not to scale.**

**Supertex Doc. #:** DSPD-3TO252K4, Version F040910.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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