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NTE7175 Integrated Circuit Quad EIA-422 Line Driver With Three-State Outputs

Description:

The NTE7175 is a Quad EIA-422 Driver in a 16-Lead DIP type package that features four independent driver chains which comply with EIA Standards for the Electrical Characteristics of Balanced Voltage Digital Interface Circuits. The outputs are three-state structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. All input pins are PNP buffered to minimize input loading for either logic one or logic zero inputs. In addition, internal circuitry assures a high impedance output state during the transition between power up and power down.

Features:

- Four Independent Driver Chains
- Three-State Outputs
- PNP High Impedance Inputs (PIA Compatible)
- Fast Propagation Times (Typ 15ns)
- TTL Compatible
- Single 5V Supply Voltage
- Output Rise and Fall Times Less Than 20ns

Absolute Maximum Ratings:

Power Supply Voltage, V_{CC} 8.0Vdc
 Input Voltage, V_I 5.5Vdc
 Operating Ambient Temperature Range, T_A 0° to +70°C
 Operating Junction Temperature Range, T_J +150°C
 Storage Temperature Range, T_{stg} -65° to +150°C

Electrical Characteristics: ($4.75V \leq V_{CC} \leq 5.25V$ and $0^\circ C \leq T_A \leq 70^\circ C$. Typical Values Measured at $V_{CC} = 5V$, and $T_A = +25^\circ C$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage	V_{IL}	Low Logic State	-	-	0.8	Vdc
	V_{IH}	High Logic State	2.0	-		Vdc
Input Current – Low Logic State	I_{IL}	$V_{IL} = 0.5V$	-	-	-400	μA
Input Current – High Logic State	I_{IH}	$V_{IH} = 2.7V$	-	-	+50	μA
		$V_{IH} = 5.5V$	-	-	+100	μA

Electrical Characteristics (Cont'd): ($4.75V \leq V_{CC} \leq 5.25V$ and $0^{\circ}C \leq T_A \leq 70^{\circ}C$ Typical Values Measured at $V_{CC} = 5V$, and $T_A = +25^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Clamp Voltage	V_{IK}	$I_{IK} = -18mA$	-	-	-1.5	V
Output Voltage	V_{OL}	$I_{OL} = 48mA$	-	-	0.5	V
Output Short-Circuit Current	I_{OS}	$V_{IH} = 2.0V$, Note 1	-40	-	-140	mA
Output Leakage Current – Hi-Z State	$I_{OL(Z)}$	$V_{IL} = 0.5V$, $V_{IL(Z)} = 0.8V$	-	-	± 100	μA
		$V_{IH} = 2.7V$, $V_{IL(Z)} = 0.8V$	-	-	± 100	μA
Output Leakage Current – Power OFF	$I_{OL(off)}$	$V_{OH} = 6.0V$, $V_{CC} = 0V$	-	-	+100	μA
		$V_{OL} = -0.25V$, $V_{CC} = 0V$	-	-	-100	μA
Output Offset Voltage Difference	$V_{OS} - \bar{V}_{OS}$	Note 2	-	-	± 0.4	V
Output Differential Voltage	V_{OD}	Note 2	2.0	-	-	V
Output Differential Voltage Difference	$ \Delta V_{OD} $	Note 2	-	-	± 0.4	V
Power Supply Current	I_{CCX}	Control Pins = GND, Note 3	-	-	105	mA
	I_{CC}	Control Pins = 2.0V	-	-	85	mA
Switching Characteristics ($V_{CC} = 5V$, $T_A = +25^{\circ}C$, unless otherwise specified)						
Propagation Delay Times	t_{PHL}	High to Low Output	-	-	20	ns
	t_{PLH}	Low to High Output	-	-	20	ns
Output Transition Times Differential	t_{THL}	High to Low Output	-	-	20	ns
	t_{TLH}	Low to High Output	-	-	20	ns
Propagation Delay – Control to Output	$t_{PHZ(E)}$	$R_L = 200\Omega$, $C_L = 50pF$	-	-	25	ns
	$t_{PLZ(E)}$	$R_L = 200\Omega$, $C_L = 50pF$	-	-	25	ns
	$t_{PZH(E)}$	$R_L = \infty$, $C_L = 50pF$	-	-	30	ns
	$t_{PZL(E)}$	$R_L = 200\Omega$, $C_L = 50pF$	-	-	30	ns

Note 1 Only one output may be stored at a time

Note 2 See EIA Specification EIA-422 for exact test conditions

Note 3 Circuit in three-state condition

Truth Table:

Input	Control Input	Non-Inverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low Logic State

H = High Logic State

X = Irrelevant

Z = Third-State (High Impedance)

Pin Connection Diagram

