DS75176B/DS75176BT Multipoint RS-485/RS-422 Transceivers

Check for Samples: DS75176B, DS75176BT

FEATURES

- **Meets EIA Standard RS485 for Multipoint Bus Transmission and is Compatible with RS-422.**
- **Small Outline (SOIC) Package Option Available for Minimum Board Space.**
- **22 ns Driver Propagation Delays.**
- **Single +5V Supply.**
- **−7V to +12V Bus Common Mode Range Permits ±7V Ground Difference Between Devices on the Bus.**
- **Thermal Shutdown Protection.**
- **High Impedance to Bus with Driver in TRI-STATE or with Power Off, Over the Entire Common Mode Range Allows the Unused Devices on the Bus to be Powered Down.**
- **Pin Out Compatible with DS3695/A and SN75176A/B.**
- **Combined Impedance of a Driver Output and Receiver Input is Less Than One RS485 Unit Load, Allowing up to 32 Transceivers on the Bus.**
- **70 mV Typical Receiver Hysteresis.**

DESCRIPTION

The DS75176B is a high speed differential TRI-STATE®bus/line transceiver designed to meet the requirements of EIA standard RS485 with extended common mode range (+12V to −7V), for multipoint data transmission. In addition, it is compatible with RS-422.

The driver and receiver outputs feature TRI-STATE capability, for the driver outputs over the entire common mode range of +12V to −7V. Bus contention or fault situations that cause excessive power dissipation within the device are handled by a thermal shutdown circuit, which forces the driver outputs into the high impedance state.

DC specifications are guaranteed over the 0 to 70°C temperature and 4.75V to 5.25V supply voltage range.

Connection and Logic Diagram

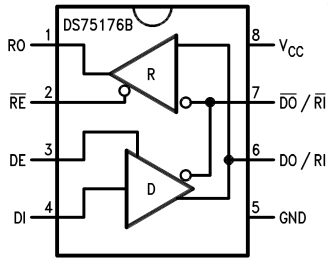


Figure 1. Top View
See Package Number P0008E or D0008A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Supply Voltage, V_{CC}		7V
Control Input Voltages		7V
Driver Input Voltage		7V
Driver Output Voltages		+15V/ −10V
Receiver Input Voltages (DS75176B)		+15V/ −10V
Receiver Output Voltage		5.5V
Continuous Power Dissipation @ 25°C	for SOIC Package	675 mW (3)
	for PDIP Package	900 mW (4)
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)		260°C
ESD Rating (HBM)		500V

(1) "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be verified. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Derate linearly @ 6.11 mW/°C to 400 mW at 70°C.
(4) Derate linearly at 5.56 mW/°C to 650 mW at 70°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Voltage at Any Bus Terminal (Separate or Common Mode)	−7	+12	V
Operating Free Air Temperature T_A			
DS75176B	0	+70	°C
DS75176BT	−40	+85	°C
Differential Input Voltage, VID (1)	−12	+12	V

(1) Differential - Input/Output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

Electrical Characteristics (1) (2)

0°C ≤ T_A ≤ 70°C, 4.75V < V_{CC} < 5.25V unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OD1}	Differential Driver Output Voltage (Unloaded)	I_O = 0				5	V
V_{OD2}	Differential Driver Output Voltage (with Load)	See (Figure 2)	R = 50Ω; (RS-422) (3)	2			V
			R = 27Ω; (RS-485)	1.5			V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage For Complementary Output States	See (Figure 2)	R = 27Ω			0.2	V
V_{OC}	Driver Common Mode Output Voltage					3.0	V
$\Delta\lvert V_{OC}\rvert$	Change in Magnitude of Driver Common Mode Output Voltage For Complementary Output States					0.2	V

(1) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
(2) All typicals are given for V_{CC} = 5V and T_A = 25°C.
(3) All worst case parameters for which this note is applied, must be increased by 10% for DS75176BT. The other parameters remain valid for −40°C < T_A < +85°C.

Electrical Characteristics (1) (2) (continued)

0°C ≤ T_A ≤ 70°C, 4.75V < V_{CC} < 5.25V unless otherwise specified

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_{IH}	Input High Voltage	DI, DE, $\overline{RE}$, E			2			V
V_{IL}	Input Low Voltage						0.8	
V_{CL}	Input Clamp Voltage			I_{IN} = −18 mA			−1.5	
I_{IL}	Input Low Current			V_{IL} = 0.4V			−200	µA
I_{IH}	Input High Current			V_{IH} = 2.4V			20	µA
I_{IN}	Input Current	DO/RI, $\overline{DO}$/$\overline{RI}$	V_{CC} = 0V or 5.25V	V_{IN} = 12V			+1.0	mA
			DE = 0V	V_{IN} = −7V			−0.8	mA
V_{TH}	Differential Input Threshold Voltage for Receiver		−7V ≤ V_{CM} ≤ + 12V		−0.2		+0.2	V
ΔV_{TH}	Receiver Input Hysteresis		V_{CM} = 0V			70		mV
V_{OH}	Receiver Output High Voltage		I_{OH} = −400 µA		2.7			V
V_{OL}	Output Low Voltage	RO	I_{OL} = 16 mA (3)				0.5	V
I_{OZR}	OFF-State (High Impedance) Output Current at Receiver		V_{CC} = Max 0.4V ≤ V_O ≤ 2.4V				±20	µA
R_{IN}	Receiver Input Resistance		−7V ≤ V_{CM} ≤ +12V		12			kΩ
I_{CC}	Supply Current		No Load (3)	Driver Outputs Enabled			55	mA
				Driver Outputs Disabled			35	mA
I_{OSD}	Driver Short-Circuit Output Current		V_O = −7V (3)				−250	mA
			V_O = +12V (3)				+250	mA
I_{OSR}	Receiver Short-Circuit Output Current		V_O = 0V		−15		−85	mA

Switching Characteristics

V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Driver Input to Output	R_{LDIFF} = 60Ω		12	22	ns
t_{PHL}	Driver Input to Output	C_{L1} = C_{L2} = 100 pF		17	22	ns
t_r	Driver Rise Time	R_{LDIFF} = 60Ω			18	ns
t_f	Driver Fall Time	C_{L1} = C_{L2} = 100 pF (Figure 4 and Figure 6)			18	ns
t_{ZH}	Driver Enable to Output High	C_L = 100 pF (Figure 5 and Figure 7) S1 Open		29	100	ns
t_{ZL}	Driver Enable to Output Low	C_L = 100 pF (Figure 5 and Figure 7) S2 Open		31	60	ns
t_{LZ}	Driver Disable Time from Low	C_L = 15 pF (Figure 5 and Figure 7) S2 Open		13	30	ns
t_{HZ}	Driver Disable Time from High	C_L = 15 pF (Figure 5 and Figure 7) S1 Open		19	200	ns
t_{PLH}	Receiver Input to Output	C_L = 15 pF (Figure 3 and Figure 8) S1 and S2 Closed		30	37	ns
t_{PHL}	Receiver Input to Output			32	37	ns
t_{ZL}	Receiver Enable to Output Low	C_L = 15 pF (Figure 3 and Figure 9) S2 Open		15	20	ns
t_{ZH}	Receiver Enable to Output High	C_L = 15 pF (Figure 3 and Figure 9) S1 Open		11	20	ns
t_{LZ}	Receiver Disable from Low	C_L = 15 pF (Figure 3 and Figure 9) S2 Open		28	32	ns
t_{HZ}	Receiver Disable from High	C_L = 15 pF (Figure 3 and Figure 9) S1 Open		13	35	ns

AC TEST CIRCUITS

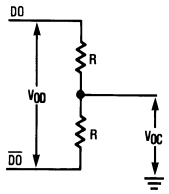
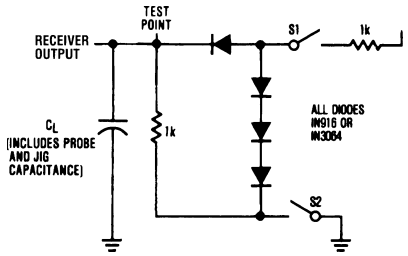


Figure 2.



Note: S1 and S2 of load circuit are closed except as otherwise mentioned.

Figure 3.

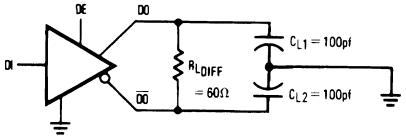
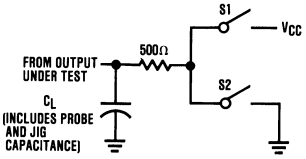


Figure 4.



Note: Unless otherwise specified the switches are closed.

Figure 5.

Switching Time Waveforms

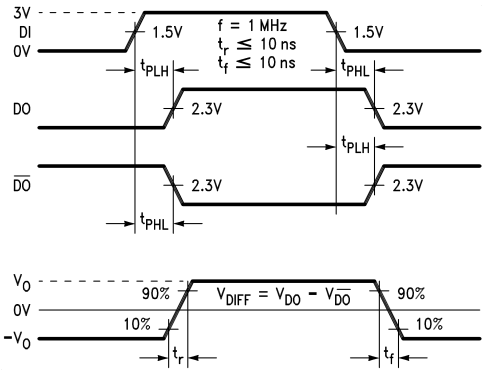


Figure 6. Driver Propagation Delays and Transition Times

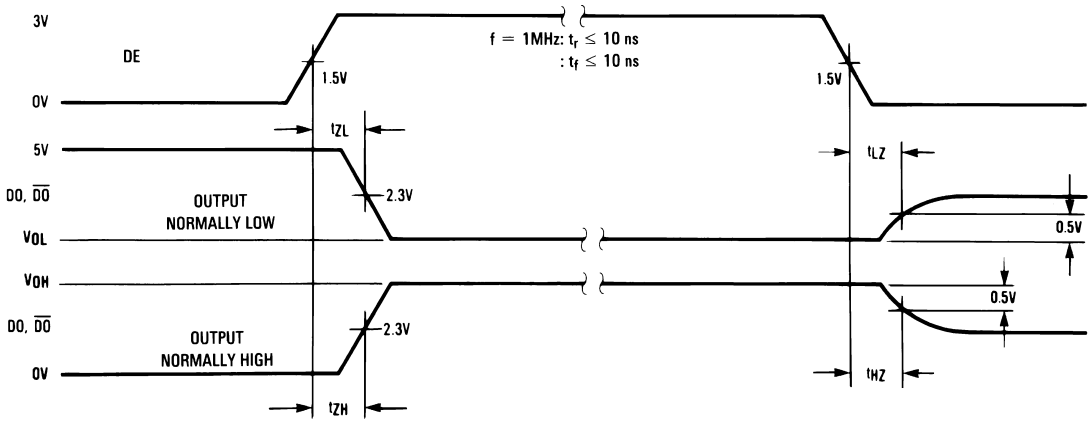
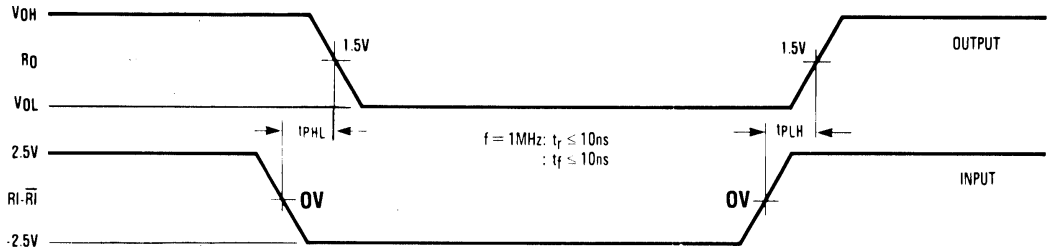


Figure 7. Driver Enable and Disable Times



Note: Differential input voltage may may be realized by grounding $\overline{RI}$ and pulsing RI between +2.5V and −2.5V

Figure 8. Receiver Propagation Delays

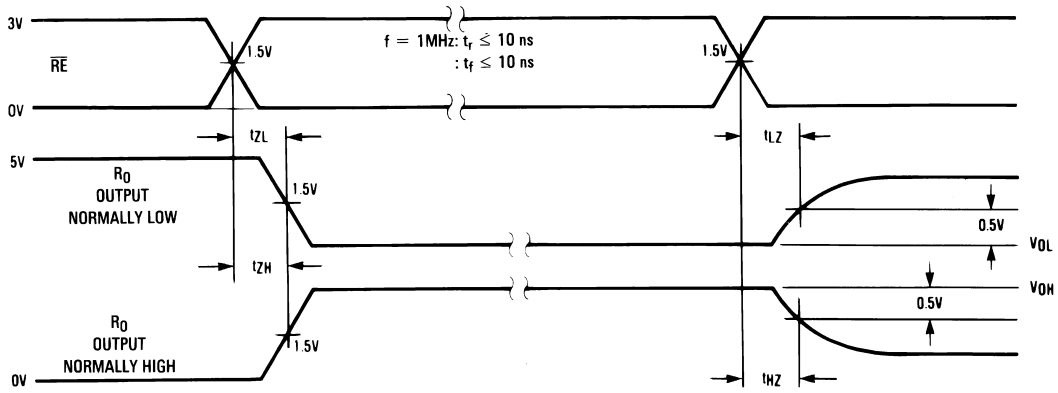


Figure 9. Receiver Enable and Disable Times

Function Tables

Table 1. DS75176B Transmitting(1)

Inputs			Line Condition	Outputs	
$\overline{RE}$	DE	DI		$\overline{DO}$	DO
X	1	1	No Fault	0	1
X	1	0	No Fault	1	0
X	0	X	X	Z	Z
X	1	X	Fault	Z	Z

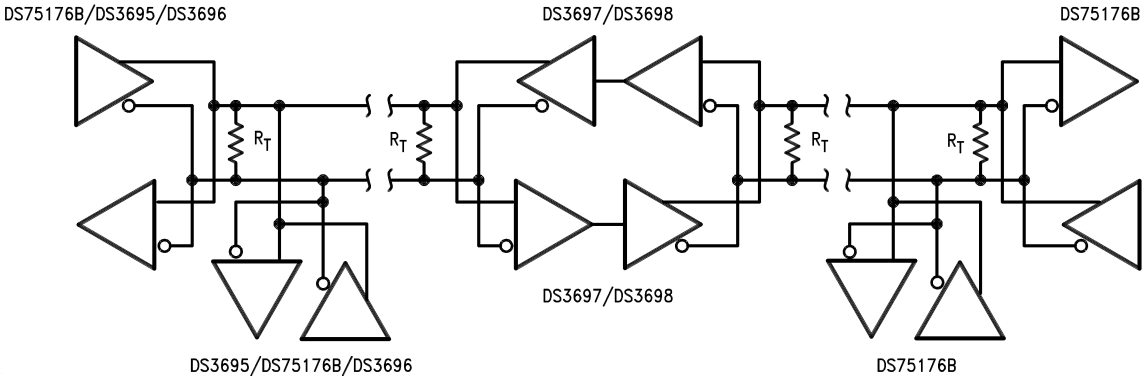
(1) X — Don't care condition
Z — High impedance state
Fault — Improper line conditons causing excessive power dissipation in the driver, such as shorts or bus contention situations
**This is a fail safe condition

Table 2. DS75176B Receiving[1]

Inputs			Outputs
$\overline{RE}$	DE	RI-$\overline{RI}$	RO
0	0	≥ +0.2V	1
0	0	≤ −0.2V	0
0	0	Inputs Open**	1
1	0	X	Z

(1) X — Don't care condition
Z — High impedance state
Fault — Improper line conditons causing excessive power dissipation in the driver, such as shorts or bus contention situations
**This is a fail safe condition

TYPICAL APPLICATION



REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS75176BM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	DS751 76BM	
DS75176BM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS751 76BM	Samples
DS75176BMX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70	DS751 76BM	
DS75176BMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS751 76BM	Samples
DS75176BN	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	0 to 70	DS75176BN	
DS75176BN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 70	DS75176BN	Samples
DS75176BTM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	DS751 76BTM	
DS75176BTM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS751 76BTM	Samples
DS75176BTMX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	DS751 76BTM	
DS75176BTMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS751 76BTM	Samples
DS75176BTN	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	-40 to 85	DS75176 BTN	
DS75176BTN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 85	DS75176 BTN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

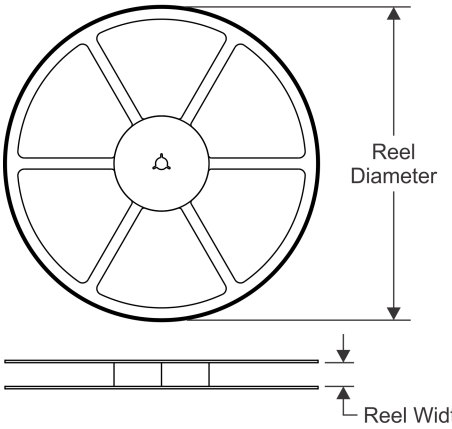
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

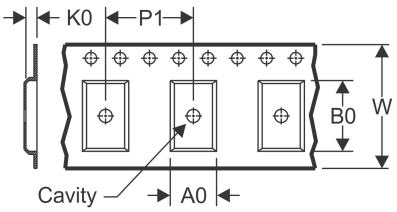
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

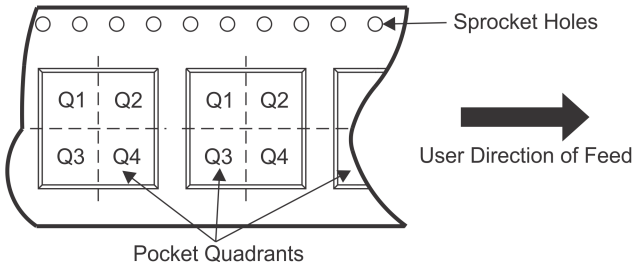


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

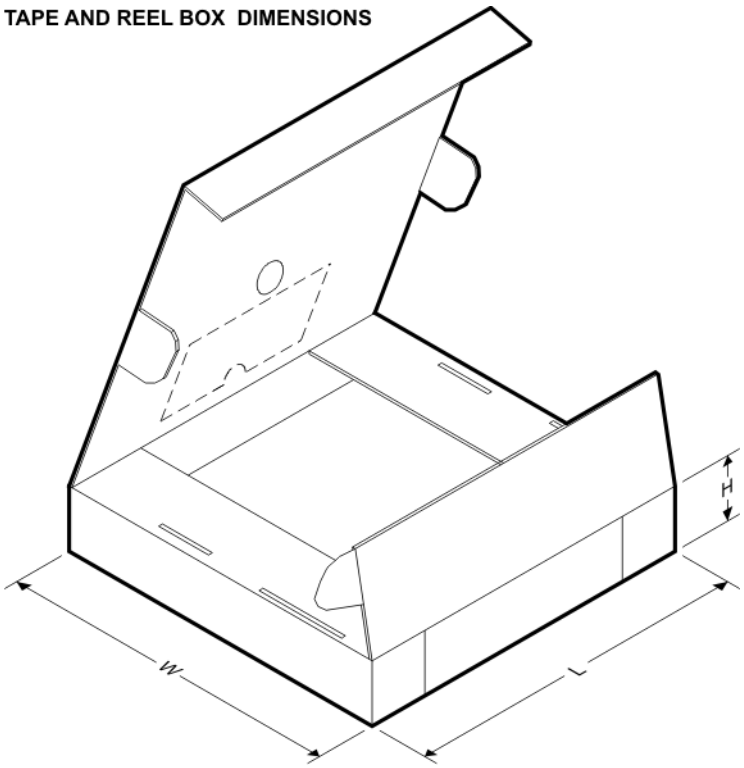
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS75176BMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
DS75176BMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
DS75176BTMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
DS75176BTMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

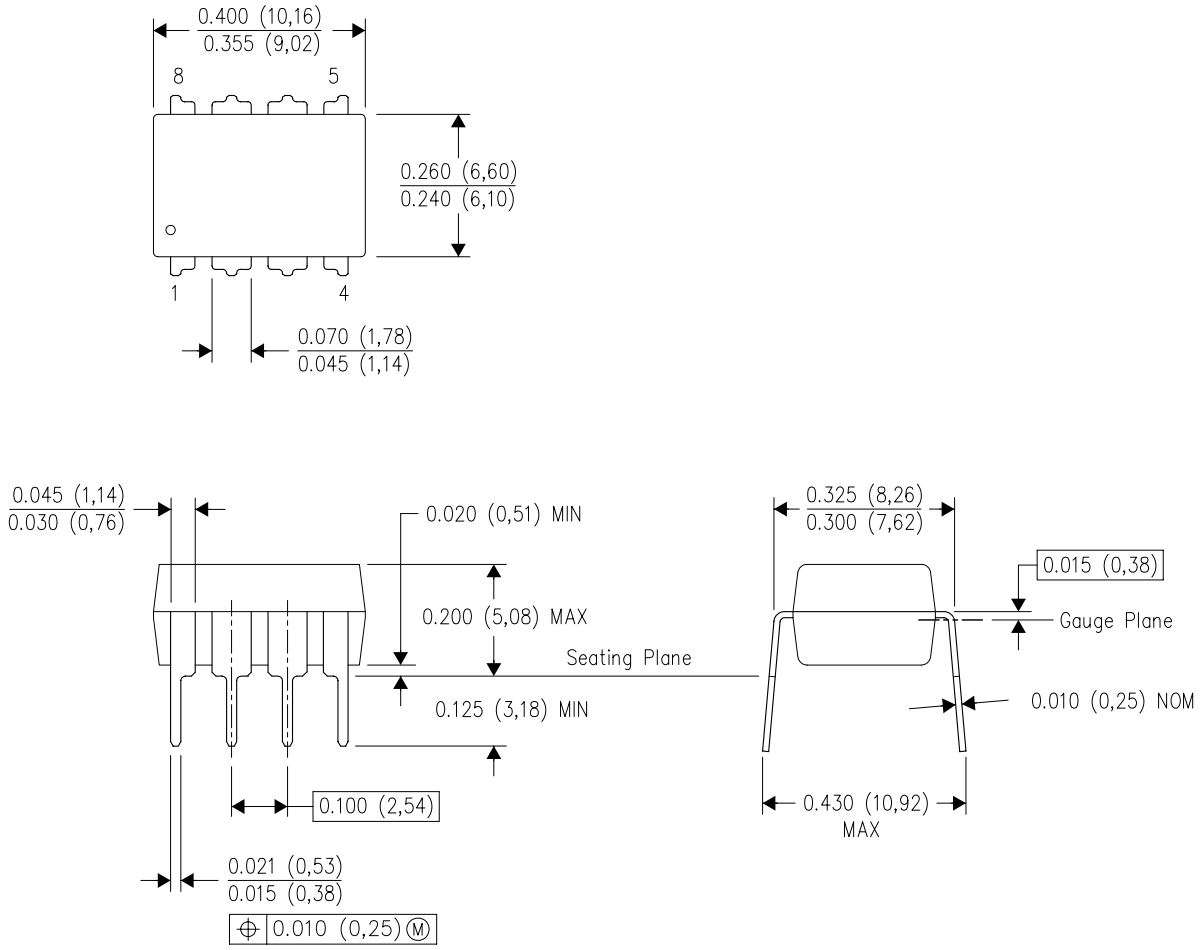
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

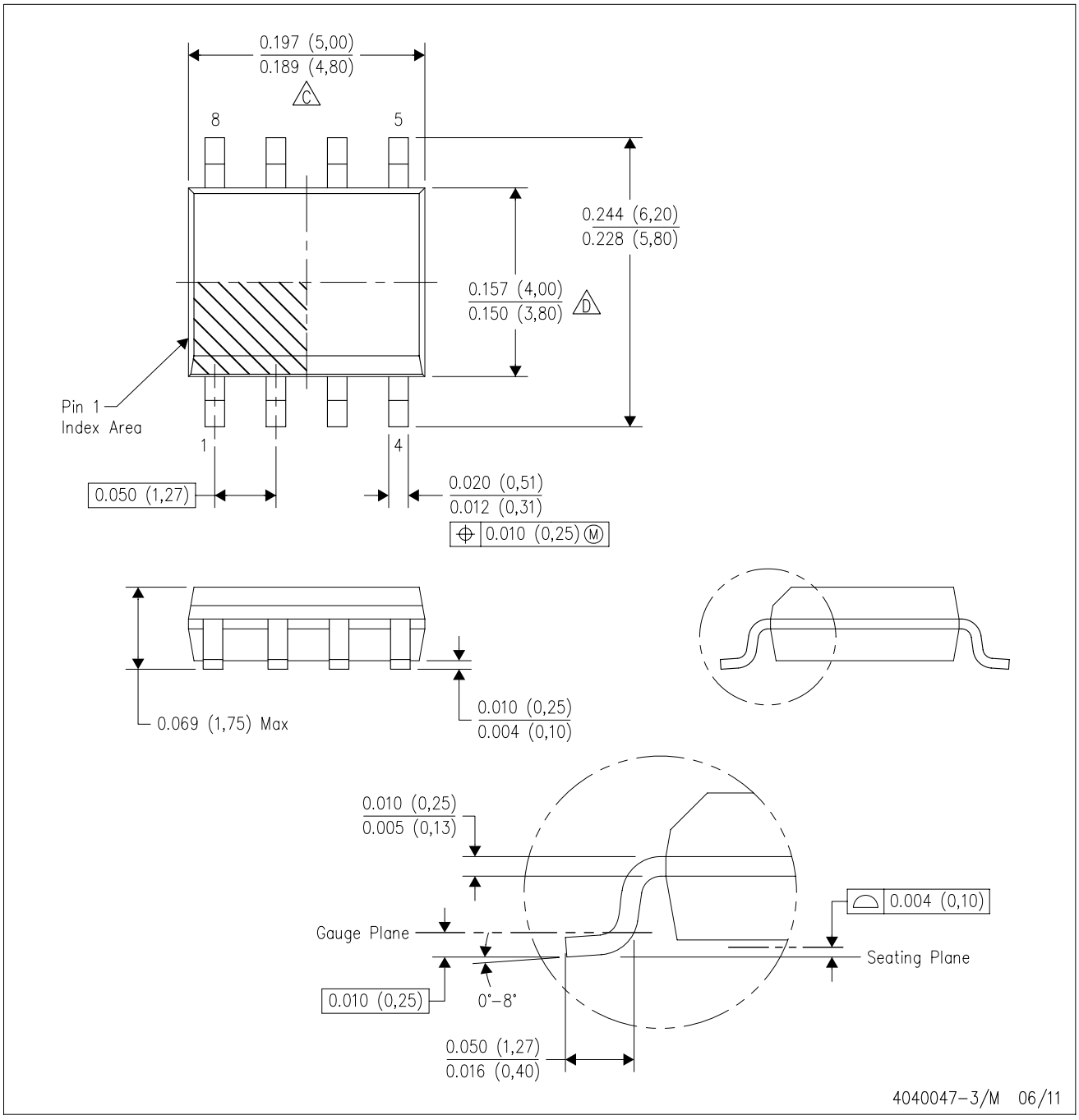
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS75176BMX	SOIC	D	8	2500	367.0	367.0	35.0
DS75176BMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
DS75176BTMX	SOIC	D	8	2500	367.0	367.0	35.0
DS75176BTMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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