LM10 Operational Amplifier and Voltage Reference

Check for Samples: LM10

FEATURES

- **Input Offset Voltage: 2 mV (max)**
- **Input Offset Current: 0.7 nA (max)**
- **Input Bias Current: 20 nA (max)**
- **Reference Regulation: 0.1% (max)**
- **Offset Voltage Drift: 2 μV/°C**
- **Reference Drift: 0.002%/°C**

DESCRIPTION

The LM10 series are monolithic linear ICs consisting of a precision reference, an adjustable reference buffer and an independent, high quality op amp.

The unit can operate from a total supply voltage as low as 1.1V or as high as 40V, drawing only 270μA. A complementary output stage swings within 15 mV of the supply terminals or will deliver ±20 mA output current with ±0.4V saturation. Reference output can be as low as 200 mV.

The circuit is recommended for portable equipment and is completely specified for operation from a single power cell. In contrast, high output-drive capability, both voltage and current, along with thermal overload protection, suggest it in demanding general-purpose applications.

The device is capable of operating in a floating mode, independent of fixed supplies. It can function as a remote comparator, signal conditioner, SCR controller or transmitter for analog signals, delivering the processed signal on the same line used to supply power. It is also suited for operation in a wide range of voltage- and current-regulator applications, from low voltages to several hundred volts, providing greater precision than existing ICs.

This series is available in the three standard temperature ranges, with the commercial part having relaxed limits. In addition, a low-voltage specification (suffix "L") is available in the limited temperature ranges at a cost savings.

Connection and Functional Diagrams

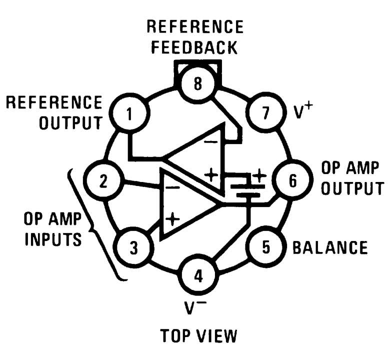


Figure 1. TO Package (NEV)
See Package Number NEV0008A

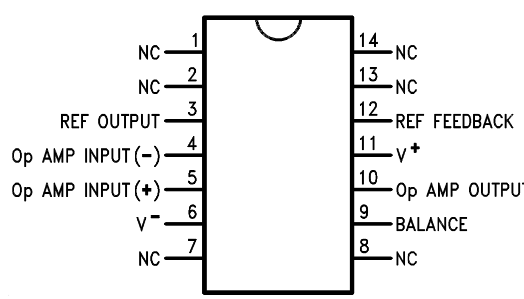


Figure 2. SOIC Package (NPA)
See Package Number NPA0014B

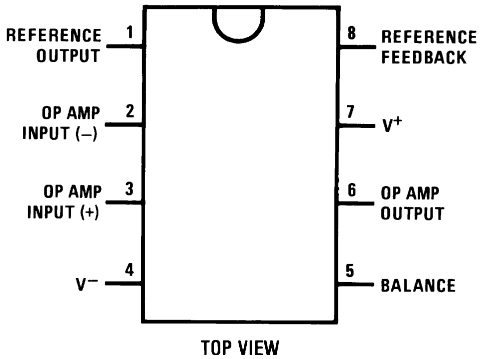


Figure 3. PDIP Package (P)
See Package Number P (R-PDIP-T8)

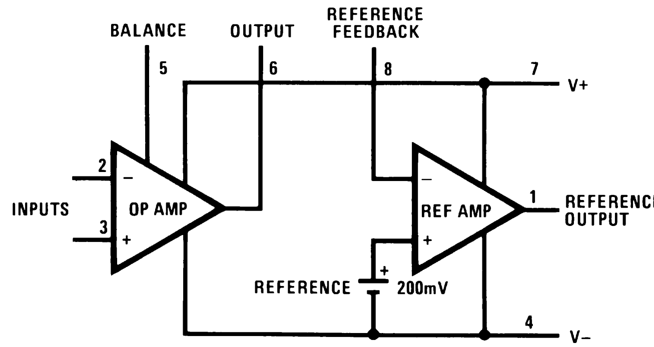


Figure 4.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

	LM10/LM10B/ LM10C	LM10BL/ LM10CL
Total Supply Voltage	45V	7V
Differential Input Voltage(4)	±40V	±7V
Power Dissipation(5)	internally limited	
Output Short-circuit Duration(6)	continuous	
Storage-Temp. Range	−55°C to +150°C	
Lead Temp. (Soldering, 10 seconds)		
TO	300°C	
Lead Temp. (Soldering, 10 seconds) DIP	260°C	
Vapor Phase (60 seconds)	215°C	
Infrared (15 seconds)	220°C	
ESD rating is to be determined.		
Maximum Junction Temperature		
LM10		150°C
LM10B		100°C
LM10C		85°C

(1) Refer to RETS10X for LM10H military specifications.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(4) The Input voltage can exceed the supply voltages provided that the voltage from the input to any other terminal does not exceed the maximum differential input voltage and excess dissipation is accounted for when $V_{IN}<V^{-}$.
(5) The maximum, operating-junction temperature is 150°C for the LM10, 100°C for the LM10B(L) and 85°C for the LM10C(L). At elevated temperatures, devices must be derated based on package thermal resistance.
(6) Internal thermal limiting prevents excessive heating that could result in sudden failure, but the IC can be subjected to accelerated stress with a shorted output and worst-case conditions.

Operating Ratings

Package Thermal Resistance	
θ_{JA}	
NEV Package	150°C/W
P Package	87°C/W
NPA Package	90°C/W
θ_{JC}	
NEV Package	45°C/W

Electrical Characteristics

T_J=25°C, **T_{MIN}≤T_J≤T_{MAX} (Boldface type refers to limits over temperature range)**(1)

Parameter	Conditions	LM10/LM10B			LM10C			Units
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage			0.3	2.0		0.5	4.0	mV
				3.0			**5.0**	mV
Input offset current(2)			0.25	0.7		0.4	2.0	nA
				1.5			**3.0**	nA
Input bias current			10	20		12	30	nA
				30			**40**	nA
Input resistance		250	500		150	400		kΩ
		150			**115**			kΩ
Large signal voltage gain	V_S=±20V, I_{OUT}=0	120	400		80	400		V/mV
	V_{OUT}=±19.95V	**80**			**50**			V/mV
	V_S=±20V, V_{OUT}=±19.4V	50	130		25	130		V/mV
	I_{OUT}=±20 mA **(±15 mA)**	**20**			**15**			V/mV
	V_S=±0.6V **(0.65V),** I_{OUT}=±2 mA	1.5	3.0		1.0	3.0		V/mV
	V_{OUT}=±0.4V **(±0.3V), V_{CM}=−0.4V**	**0.5**			**0.75**			V/mV
Shunt gain(3)	1.2V **(1.3V)** ≤V_{OUT}≤40V,	14	33		10	33		V/mV
	R_L=1.1 kΩ							
	0.1 mA≤I_{OUT}≤5 mA	**6**			**6**			V/mV
	1.5V≤V^+≤40V, R_L=250Ω	8	25		6	25		V/mV
	0.1 mA≤I_{OUT}≤20 mA	**4**			**4**			V/mV
Common-mode rejection	−20V≤V_{CM}≤19.15V **(19V)**	93	102		90	102		dB
	V_S=±20V	**87**			**87**			dB
Supply-voltage rejection	−0.2V≥V^-≥−39V	90	96		87	96		dB
	V^+=1.0V **(1.1V)**	**84**			**84**			dB
	1.0V **(1.1V)** ≤V^+≤39.8V	96	106		93	106		dB
	V^-=−0.2V	**90**			**90**			dB
Offset voltage drift			2.0			5.0		μV/°C
Offset current drift			2.0			5.0		pA/°C
Bias current drift	T_C<100°C		60			90		pA/°C
Line regulation	1.2V **(1.3V)** ≤V_S≤40V		0.001	0.003		0.001	0.008	%/V
	0≤I_{REF}≤1.0 mA, V_{REF}=200 mV			**0.006**			**0.01**	%/V

(1) These specifications apply for V^-≤V_{CM}≤V^+−0.85V **(1.0V),** 1.2V **(1.3V)** <V_S≤V_{MAX}, V_{REF}=0.2V and 0≤I_{REF}≤1.0 mA, unless otherwise specified: V_{MAX}=40V for the standard part and 6.5V for the low voltage part. Normal typeface indicates 25°C limits. **Boldface type indicates limits and altered test conditions for full-temperature-range operation;** this is −55°C to 125°C for the LM10, −25°C to 85°C for the LM10B(L) and 0°C to 70°C for the LM10C(L). The specifications do not include the effects of thermal gradients (τ_1≈20 ms), die heating (τ_2≈0.2s) or package heating. Gradient effects are small and tend to offset the electrical error (see curves).
(2) For T_J>90°C, I_{OS} may exceed 1.5 nA for V_{CM}=V^-. With T_J=125°C and V^-≤V_{CM}≤V^-+0.1V, I_{OS}≤5 nA.
(3) This defines operation in floating applications such as the bootstrapped regulator or two-wire transmitter. Output is connected to the V^+ terminal of the IC and input common mode is referred to V^- (see Typical Applications). Effect of larger output-voltage swings with higher load resistance can be accounted for by adding the positive-supply rejection error.

Electrical Characteristics (continued)

T_J=25°C, **T_{MIN}≤T_J≤T_{MAX} (Boldface type refers to limits over temperature range)**[1]

Parameter	Conditions	LM10/LM10B			LM10C			Units
		Min	Typ	Max	Min	Typ	Max	
Load regulation	0≤I_{REF}≤1.0 mA		0.01	0.1		0.01	0.15	%
	V^+−V_{REF}≥1.0V **(1.1V)**			**0.15**			**0.2**	%
Amplifier gain	0.2V≤V_{REF}≤35V	50	75		25	70		V/mV
		23			**15**			V/mV
Feedback sense voltage		195	200	205	190	200	210	mV
		194		**206**	**189**		**211**	mV
Feedback current			20	50		22	75	nA
				65			**90**	nA
Reference drift			0.002			0.003		%/°C
Supply current			270	400		300	500	μA
				500			**570**	μA
Supply current change	1.2V **(1.3V)** ≤V_S≤40V		15	**75**		15	**75**	μA

Electrical Characteristics

T_J=25°C, **T_{MIN}≤T_J≤T_{MAX} (Boldface type refers to limits over temperature range)**[1]

Parameter	Conditions	LM10BL			LM10CL			Units
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage			0.3	2.0		0.5	4.0	mV
				3.0			**5.0**	mV
Input offset current[2]			0.1	0.7		0.2	2.0	nA
				1.5			**3.0**	nA
Input bias current			10	20		12	30	nA
				30			**40**	nA
Input resistance		250	500		150	400		kΩ
		150			**115**			kΩ
Large signal voltage gain	V_S=±3.25V, I_{OUT}=0	60	300		40	300		V/mV
	V_{OUT}=±3.2V	**40**			**25**			V/mV
	V_S=±3.25V, I_{OUT}=10 mA	10	25		5	25		V/mV
	V_{OUT}=±2.75 V	**4**			**3**			V/mV
	V_S=±0.6V **(0.65V),** I_{OUT}=±2 mA	1.5	3.0		1.0	3.0		V/mV
	V_{OUT}=±0.4V **(±0.3V),** V_{CM}=−0.4V	**0.5**			**0.75**			V/mV
Shunt gain[3]	1.5V≤V^+≤6.5V, R_L=500Ω	8	30		6	30		V/mV
	0.1 mA≤I_{OUT}≤10 mA	**4**			**4**			V/mV
Common-mode rejection	−3.25V≤V_{CM}≤2.4V **(2.25V)**	89	102		80	102		dB
	V_S=±3.25V	**83**			**74**			dB
Supply-voltage rejection	−0.2V≥V^-≥−5.4V	86	96		80	96		dB
	V^+=1.0V **(1.2V)**	**80**			**74**			dB
	1.0V **(1.1V)** ≤V^+≤6.3V	94	106		80	106		dB
	V^-=0.2V	**88**			**74**			dB

(1) These specifications apply for V^-≤V_{CM}≤V^+−0.85V **(1.0V),** 1.2V **(1.3V)** <V_S≤V_{MAX}, V_{REF}=0.2V and 0≤I_{REF}≤1.0 mA, unless otherwise specified: V_{MAX}=40V for the standard part and 6.5V for the low voltage part. Normal typeface indicates 25°C limits. **Boldface type indicates limits and altered test conditions for full-temperature-range operation;** this is −55°C to 125°C for the LM10, −25°C to 85°C for the LM10B(L) and 0°C to 70°C for the LM10C(L). The specifications do not include the effects of thermal gradients (τ_1≃20 ms), die heating (τ_2≃0.2s) or package heating. Gradient effects are small and tend to offset the electrical error (see curves).
(2) For T_J>90°C, I_{OS} may exceed 1.5 nA for V_{CM}=V^-. With T_J=125°C and V^-≤V_{CM}≤V^-+0.1V, I_{OS}≤5 nA.
(3) This defines operation in floating applications such as the bootstrapped regulator or two-wire transmitter. Output is connected to the V^+ terminal of the IC and input common mode is referred to V^- (see Typical Applications). Effect of larger output-voltage swings with higher load resistance can be accounted for by adding the positive-supply rejection error.

Electrical Characteristics (continued)

T_J=25°C, **T_{MIN}≤T_J≤T_{MAX} (Boldface type refers to limits over temperature range)**(1)

Parameter	Conditions	LM10BL			LM10CL			Units
		Min	Typ	Max	Min	Typ	Max	
Offset voltage drift			2.0			5.0		μV/°C
Offset current drift			2.0			5.0		pA/°C
Bias current drift			60			90		pA/°C
Line regulation	1.2V **(1.3V)** ≤V_S≤6.5V		0.001	0.01		0.001	0.02	%/V
	0≤I_{REF}≤0.5 mA, V_{REF}=200 mV			**0.02**			**0.03**	%/V
Load regulation	0≤I_{REF}≤0.5 mA		0.01	0.1		0.01	0.15	%
	V^+−V_{REF}≥1.0V **(1.1V)**			**0.15**			**0.2**	%
Amplifier gain	0.2V≤V_{REF}≤5.5V	30	70		20	70		V/mV
		20			**15**			V/mV
Feedback sense voltage		195	200	205	190	200	210	mV
		194		**206**	**189**		**211**	mV
Feedback current			20	50		22	75	nA
				65			**90**	nA
Reference drift			0.002			0.003		%/°C
Supply current			260	400		280	500	μA
				500			**570**	μA

Definition of Terms

Input offset voltage: That voltage which must be applied between the input terminals to bias the unloaded output in the linear region.

Input offset current: The difference in the currents at the input terminals when the unloaded output is in the linear region.

Input bias current: The absolute value of the average of the two input currents.

Input resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Large signal voltage gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it.

Shunt gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it with the output tied to the V^+ terminal of the IC. The load and power source are connected between the V^+ and V^- terminals, and input common-mode is referred to the V^- terminal.

Common-mode rejection: The ratio of the input voltage range to the change in offset voltage between the extremes.

Supply-voltage rejection: The ratio of the specified supply-voltage change to the change in offset voltage between the extremes.

Line regulation: The average change in reference output voltage over the specified supply voltage range.

Load regulation: The change in reference output voltage from no load to that load specified.

Feedback sense voltage: The voltage, referred to V^-, on the reference feedback terminal while operating in regulation.

Reference amplifier gain: The ratio of the specified reference output change to the change in feedback sense voltage required to produce it.

Feedback current: The absolute value of the current at the feedback terminal when operating in regulation.

Supply current: The current required from the power source to operate the amplifier and reference with their outputs unloaded and operating in the linear range.

Typical Performance Characteristics (Op Amp)

Input Current

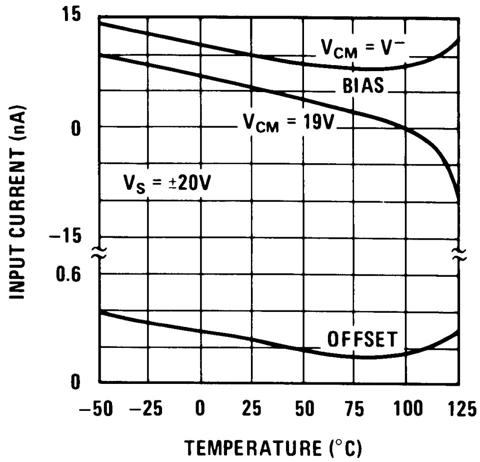


Figure 5.

Common Mode Limits

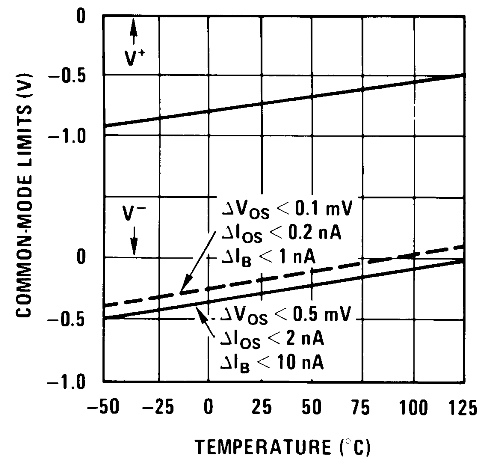


Figure 6.

Output Voltage Drift

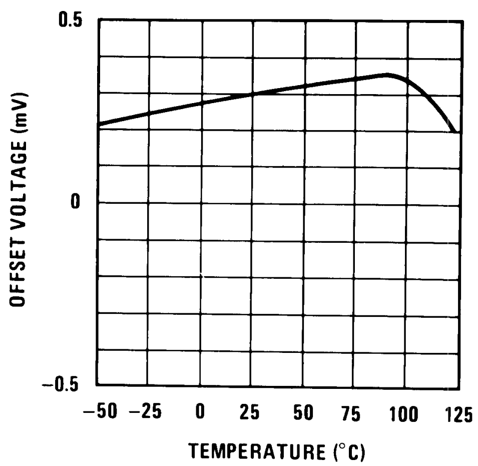


Figure 7.

Input Noise Voltage

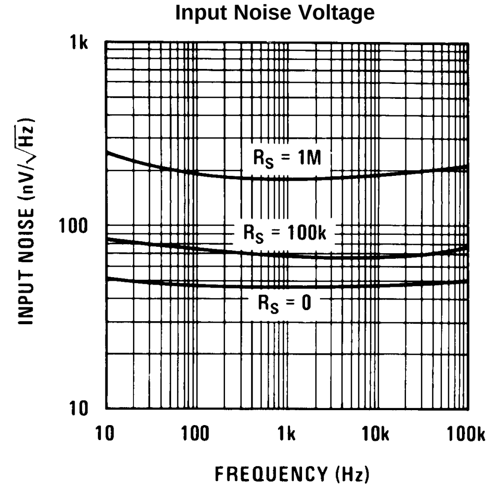


Figure 8.

DC Voltage Gain

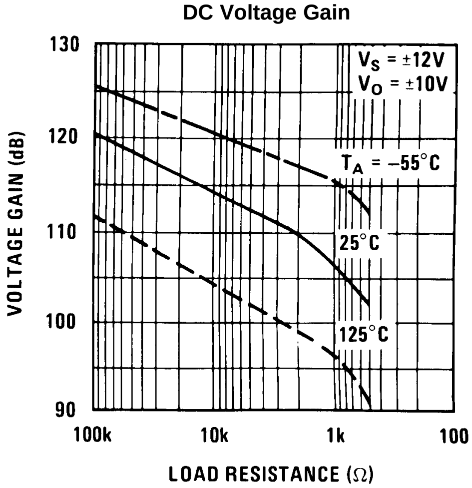


Figure 9.

Transconductance

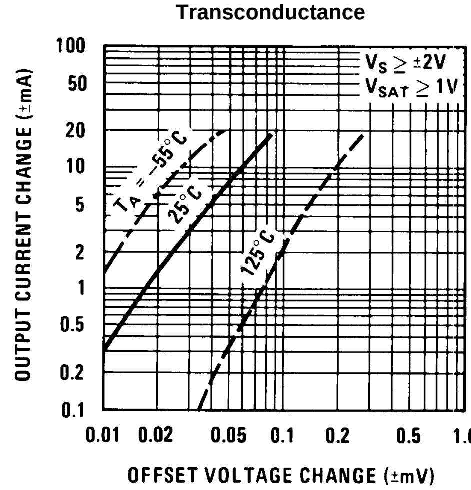


Figure 10.

Typical Performance Characteristics (Op Amp) (continued)

Output Saturation Characteristics

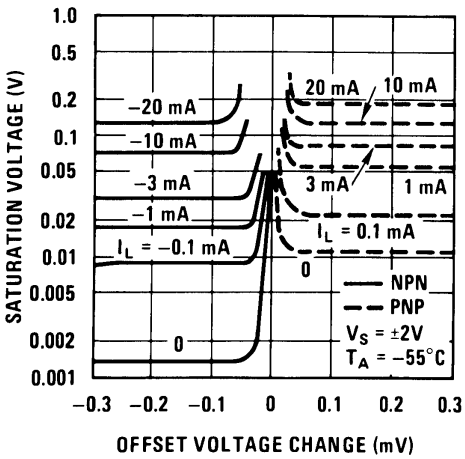


Figure 11.

Output Saturation Characteristics

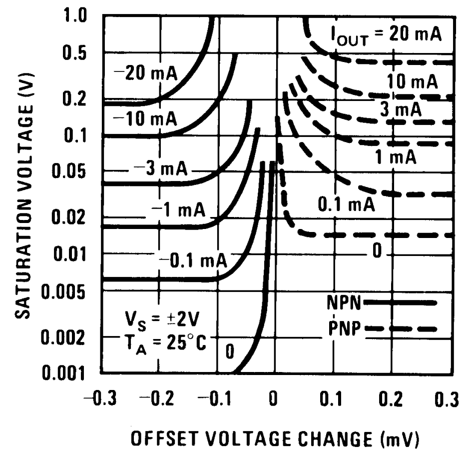


Figure 12.

Output Saturation Characteristics

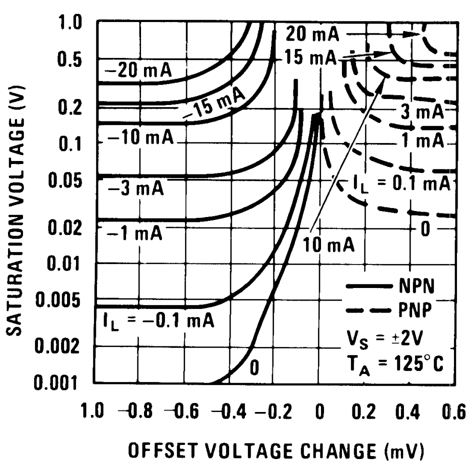


Figure 13.

Minimum Supply Voltage

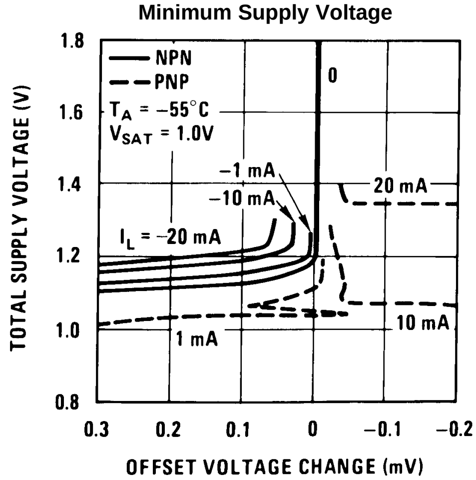


Figure 14.

Minimum Supply Voltage

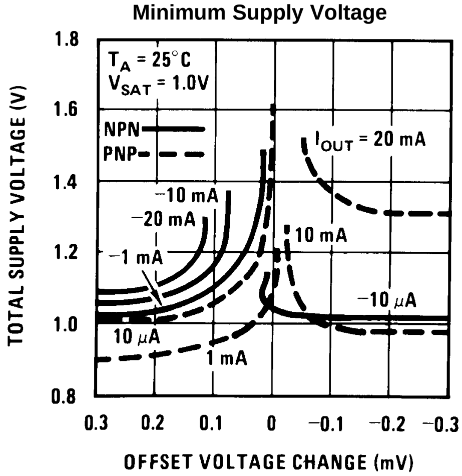


Figure 15.

Minimum Supply Voltage

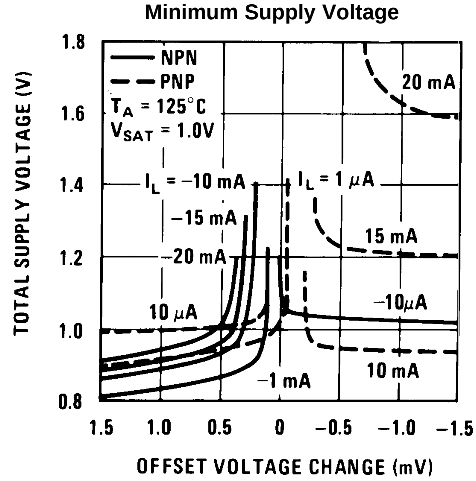


Figure 16.

Typical Performance Characteristics (Op Amp) (continued)

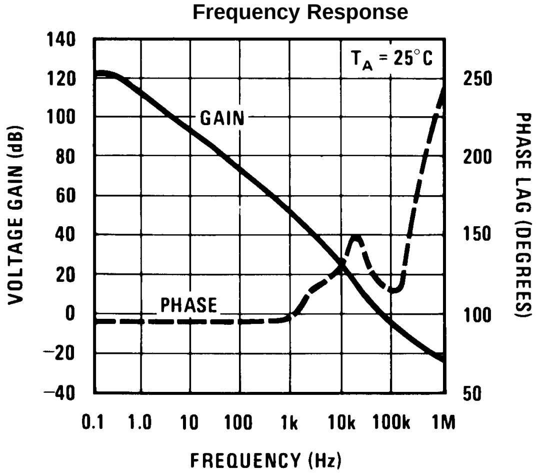


Figure 17.

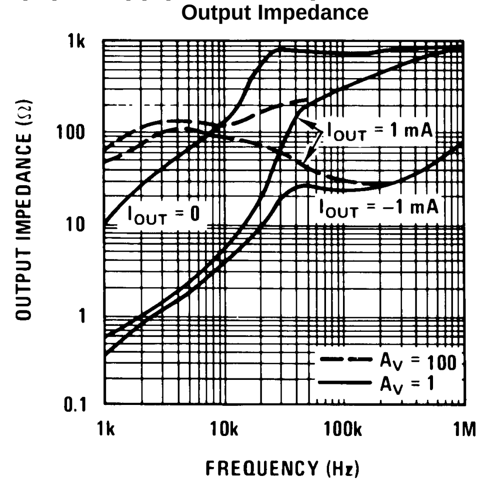


Figure 18.

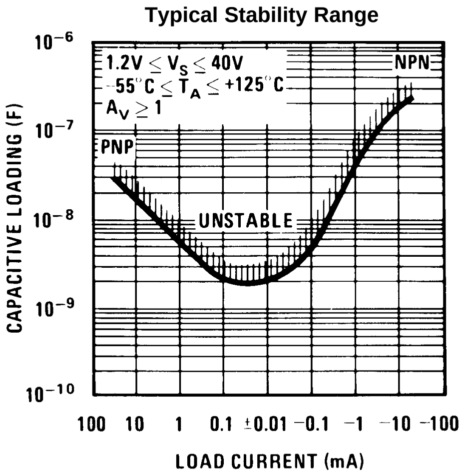


Figure 19.

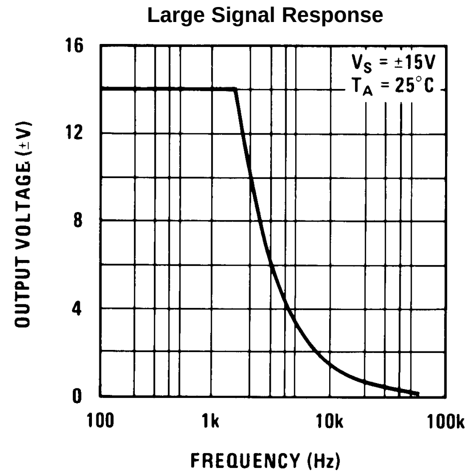


Figure 20.

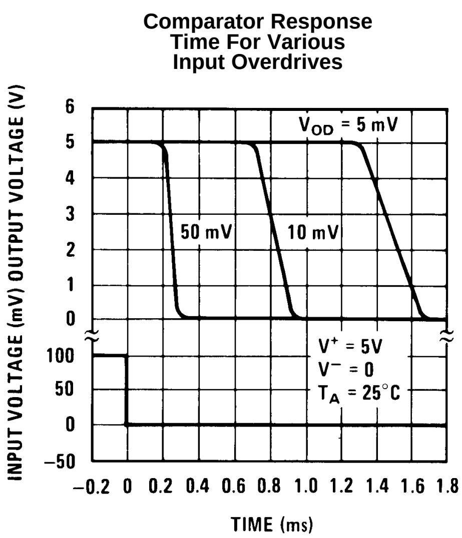


Figure 21.

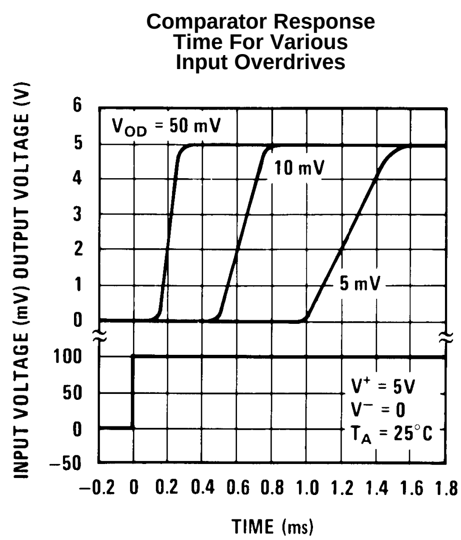


Figure 22.

Typical Performance Characteristics (Op Amp) (continued)

Follower Pulse Response

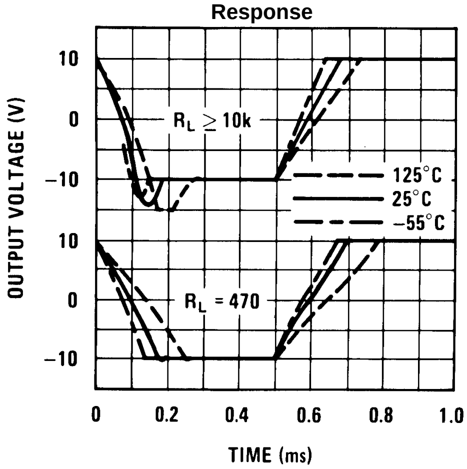


Figure 23.

Noise Rejection

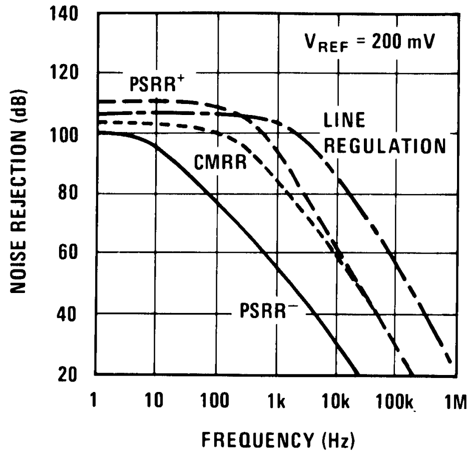


Figure 24.

Rejection Slew Limiting

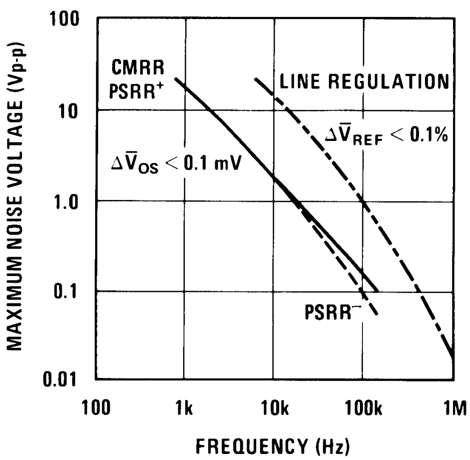


Figure 25.

Supply Current

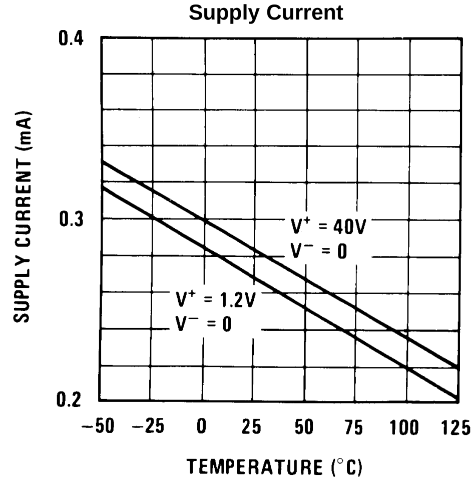


Figure 26.

Thermal Gradient Feedback

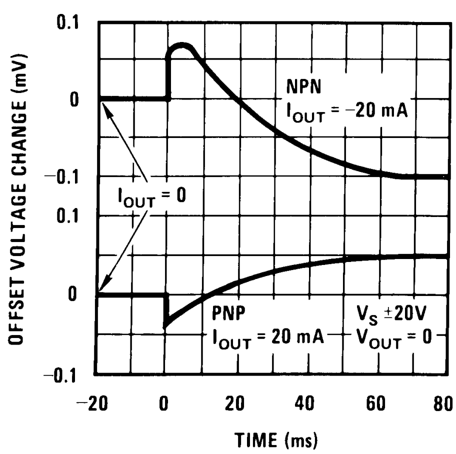


Figure 27.

Thermal Gradient Cross-coupling

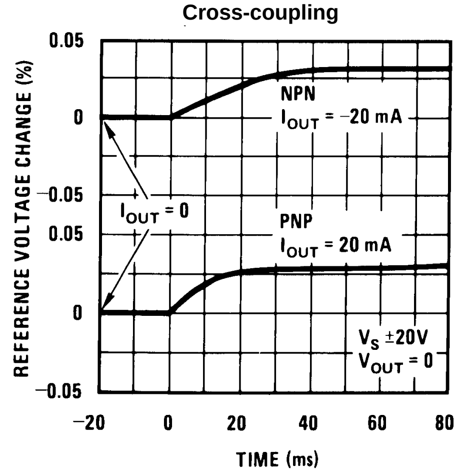


Figure 28.

Typical Performance Characteristics (Op Amp) (continued)

Shunt Gain

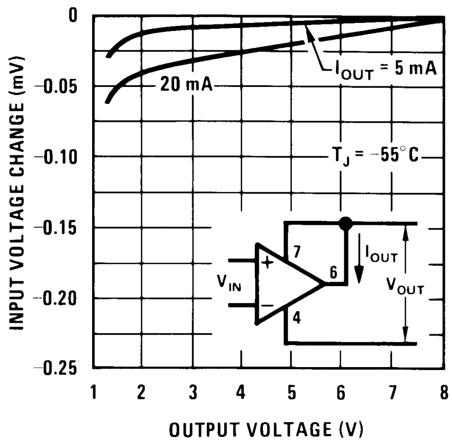


Figure 29.

Shunt Gain

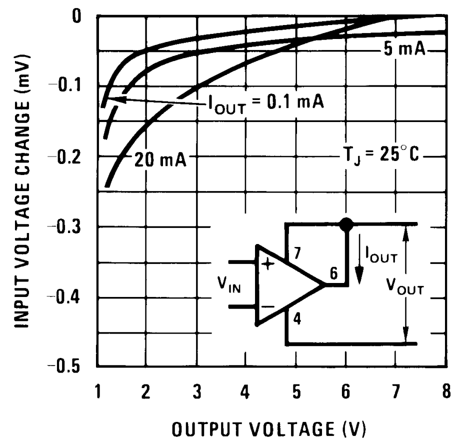


Figure 30.

Shunt Gain

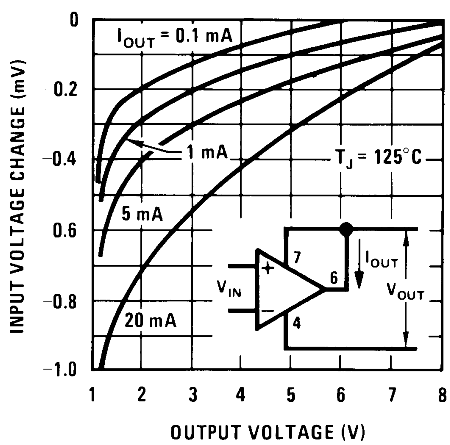


Figure 31.

Shunt Gain

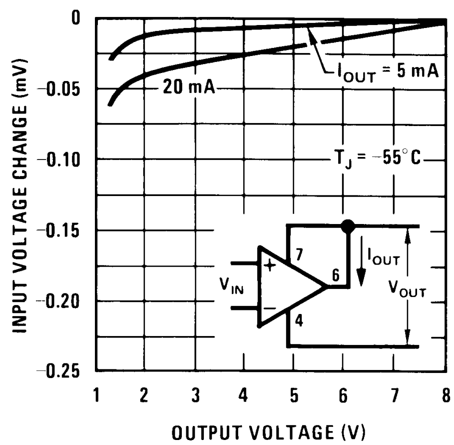


Figure 32.

Shunt Gain

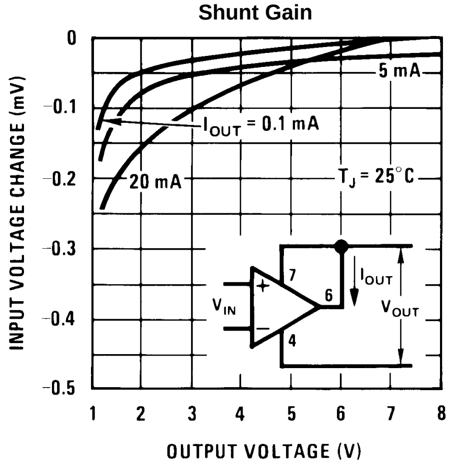


Figure 33.

Shunt Gain

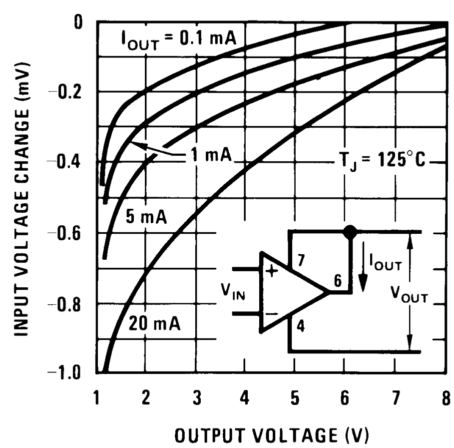


Figure 34.

Typical Performance Characteristics (Reference)

Line Regulation

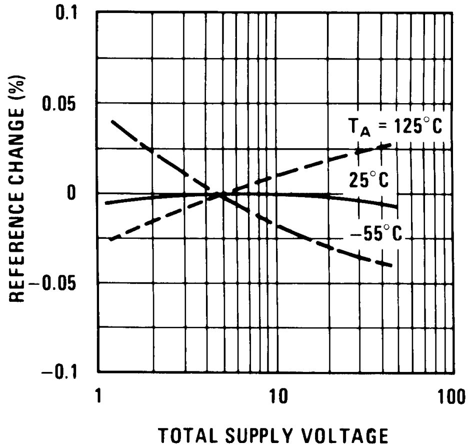


Figure 35.

Load Regulation

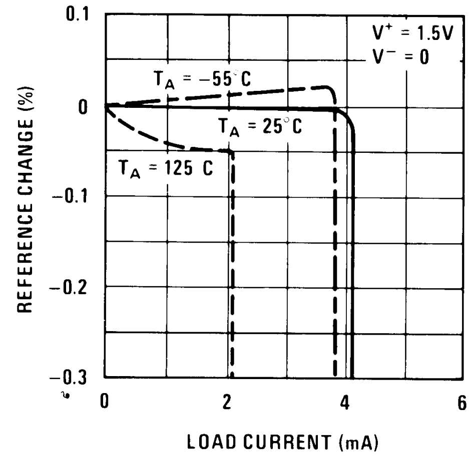


Figure 36.

Reference Noise Voltage

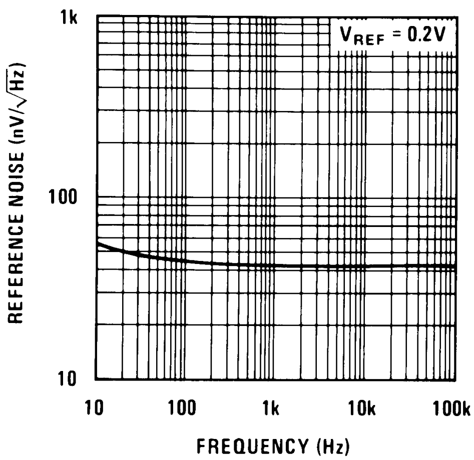


Figure 37.

Minimum Supply Voltage

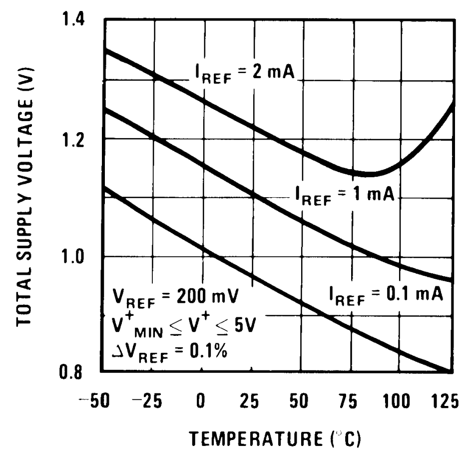


Figure 38.

Output Saturation

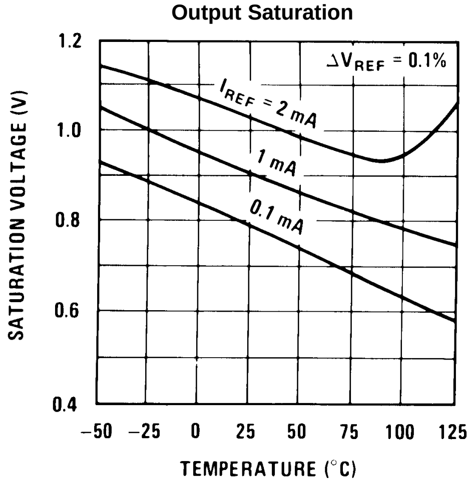


Figure 39.

Typical Stability Range

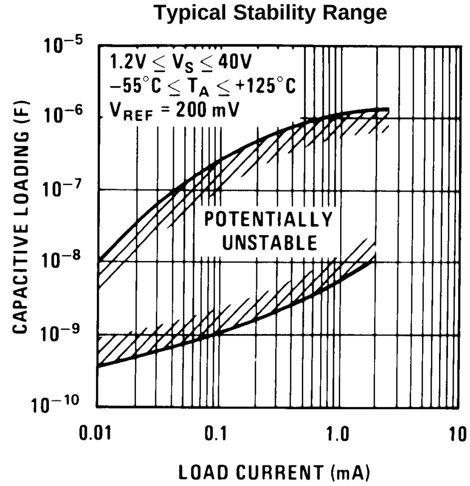


Figure 40.

TYPICAL APPLICATIONS

(Pin numbers are for devices in 8-pin packages)

Circuit descriptions available in application note AN-211 (Literature Number SNOA638).

Op Amp Offset Adjustment

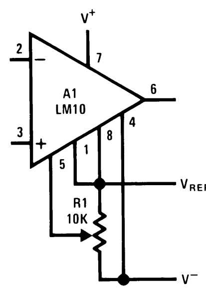


Figure 41. Standard

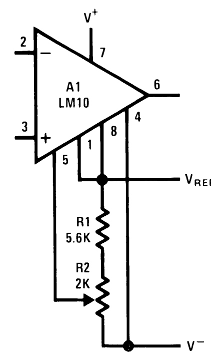


Figure 42. Limited Range

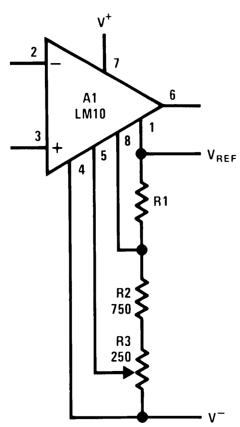


Figure 43. Limited Range With Boosted Reference

Positive Regulators

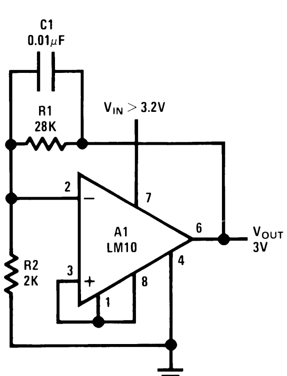


Figure 44. Low Voltage

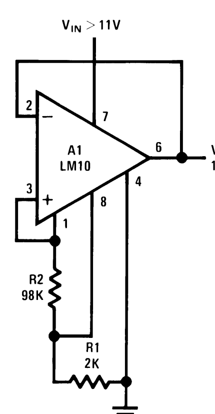
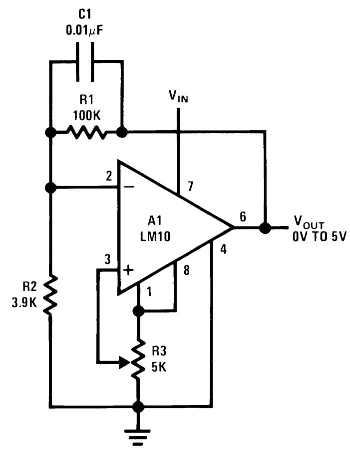


Figure 45. Best Regulation

(Pin numbers are for devices in 8-pin packages)



Use only electrolytic output capacitors.

Figure 46. Zero Output

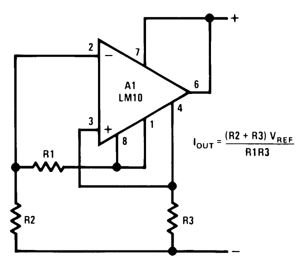
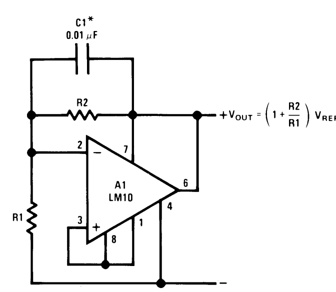


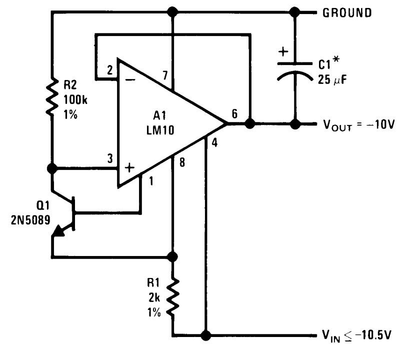
Figure 47. Current Regulator



Required For Capacitive Loading

Figure 48. Shunt Regulator

(Pin numbers are for devices in 8-pin packages)



*Electrolytic

Figure 49. Negative Regulator

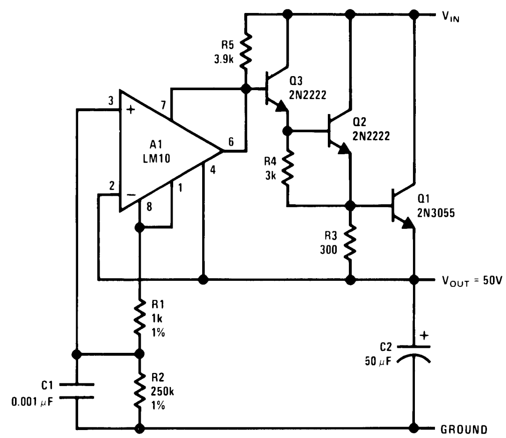
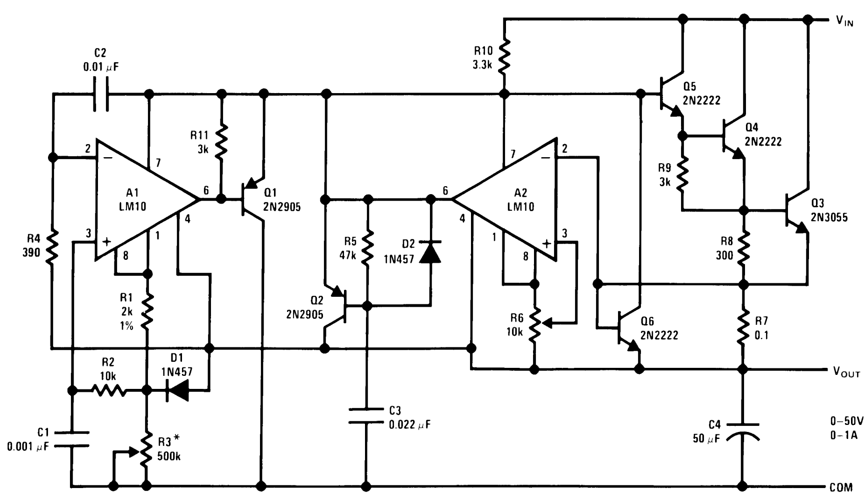


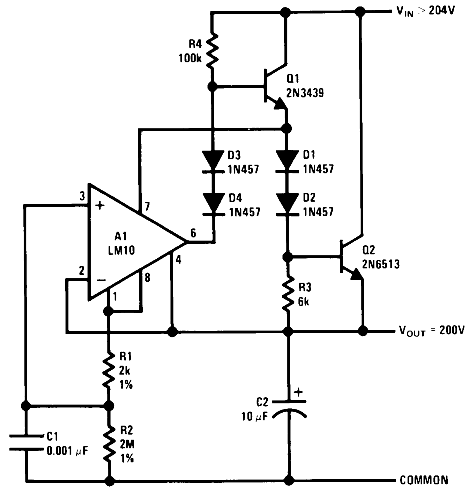
Figure 50. Precision Regulator



$^{*}V_{OUT}=10^{-4}$ R3

Figure 51. Laboratory Power Supply

(Pin numbers are for devices in 8-pin packages)



$$V_{OUT} = \frac{R2}{R1} V_{REF}$$

Figure 52. HV Regulator

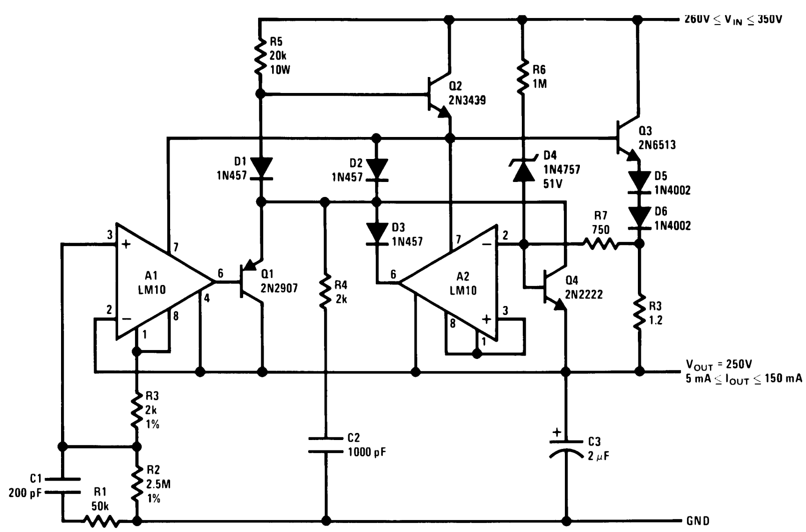
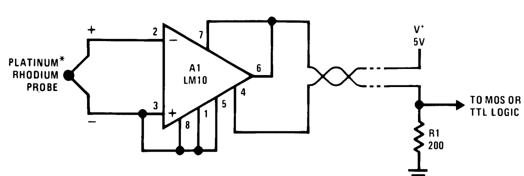


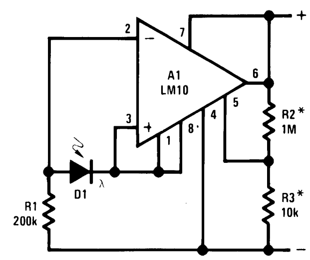
Figure 53. Protected HV Regulator



*800°C Threshold Is Established By Connecting Balance To V_{REF}.

Figure 54. Flame Detector

(Pin numbers are for devices in 8-pin packages)



*Provides Hysteresis

Figure 55. Light Level Sensor

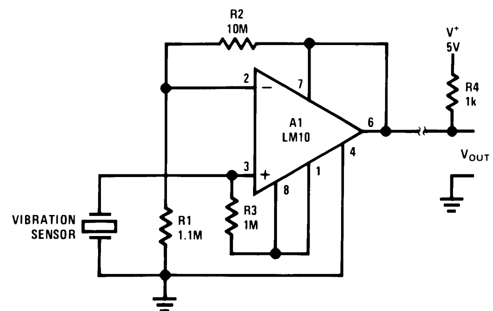


Figure 56. Remote Amplifier

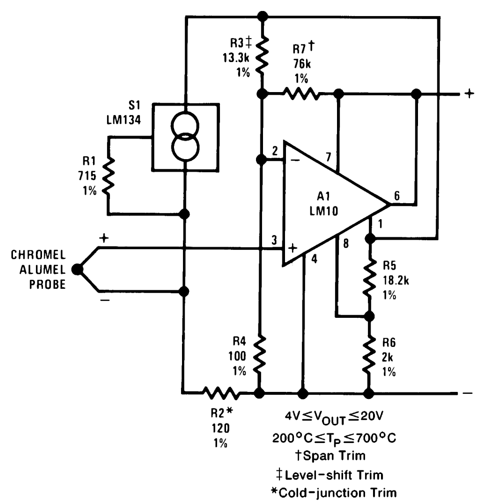


Figure 57. Remote Thermocouple Amplifier

(Pin numbers are for devices in 8-pin packages)

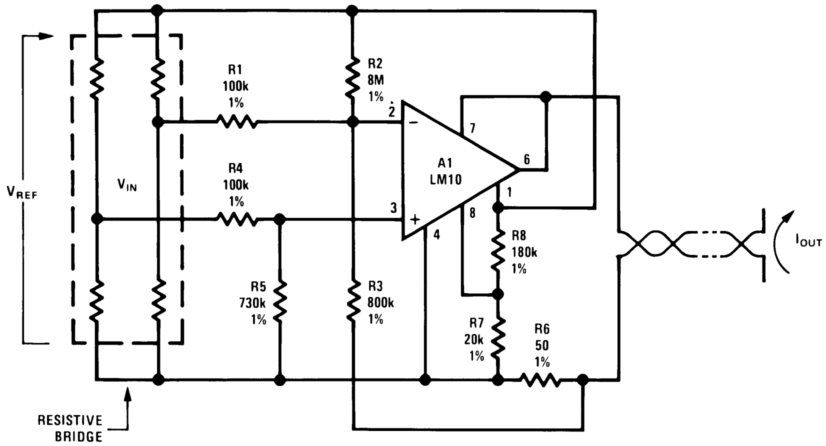
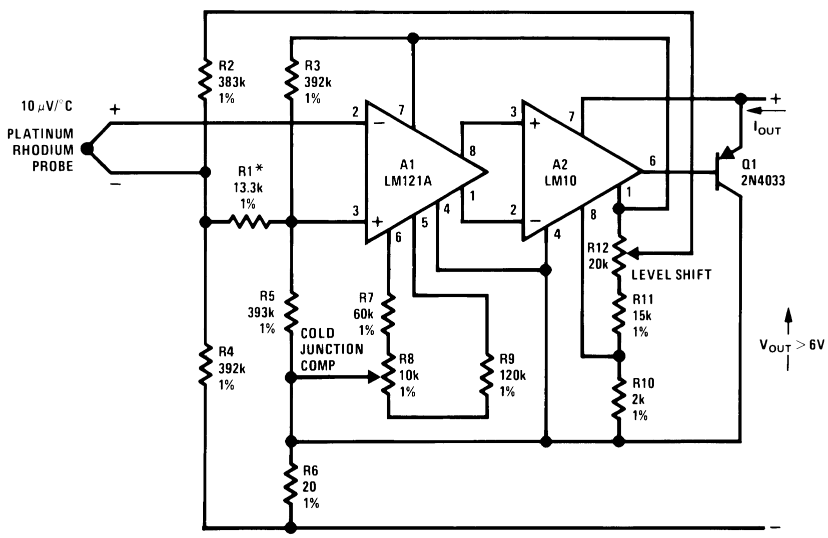


Figure 58. Transmitter for Bridge Sensor



10 mA≤I_{OUT}≤50 mA
500°C≤T_P≤1500°C
*Gain Trim

Figure 59. Precision Thermocouple Transmitter

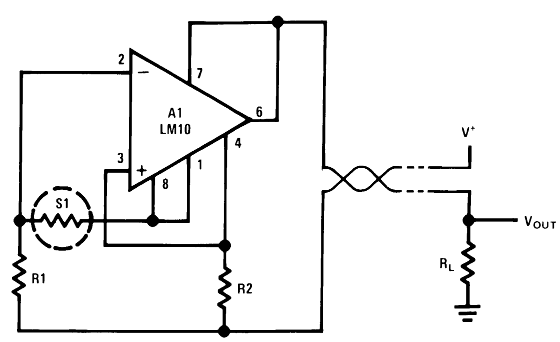
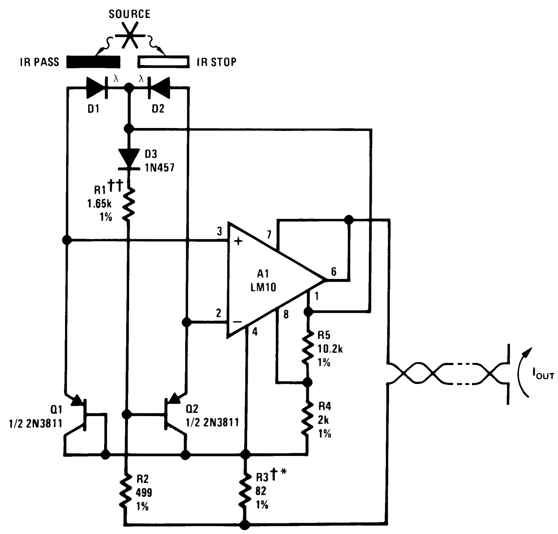


Figure 60. Resistance Thermometer Transmitter

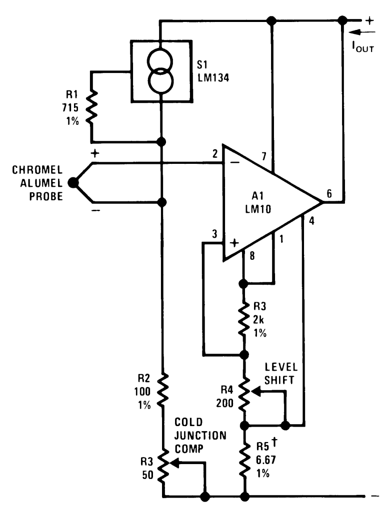
(Pin numbers are for devices in 8-pin packages)



††Level-shift Trim
*Scale Factor Trim
†Copper Wire Wound
$1 \text{ mA} \leq I_{OUT} \leq 5 \text{ mA}$

$0.01 \leq \frac{I_{D2}}{I_{D1}} \leq 100$

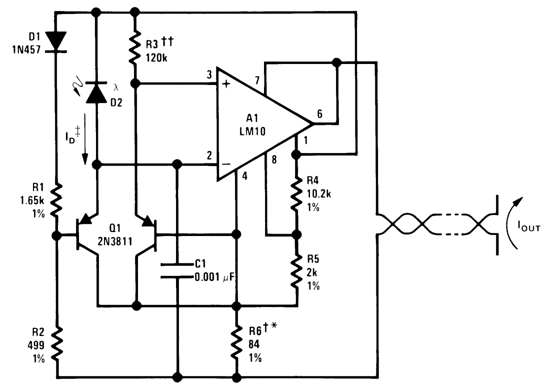
Figure 61. Optical Pyrometer



$200°C \leq T_p \leq 700°C$
$1 \text{ mA} \leq I_{OUT} \leq 5 \text{ mA}$
†Gain Trim

Figure 62. Thermocouple Transmitter

(Pin numbers are for devices in 8-pin packages)



1 mA≤I_{OUT}≤5 mA
‡50 μA≤I_D≤500 μA
††Center Scale Trim
†Scale Factor Trim
*Copper Wire Wound

Figure 63. Logarithmic Light Sensor

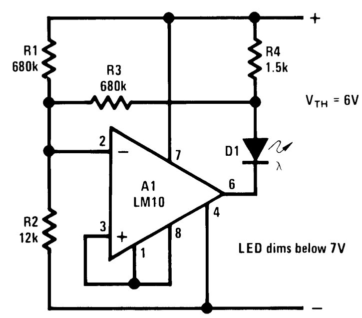


Figure 64. Battery-level Indicator

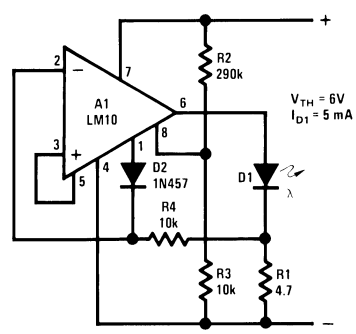
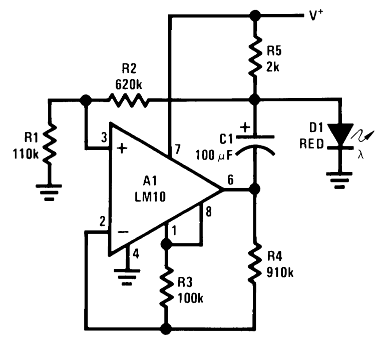


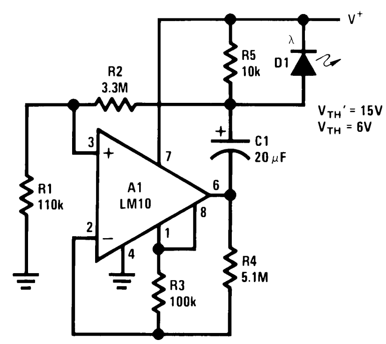
Figure 65. Battery-threshold Indicator

(Pin numbers are for devices in 8-pin packages)



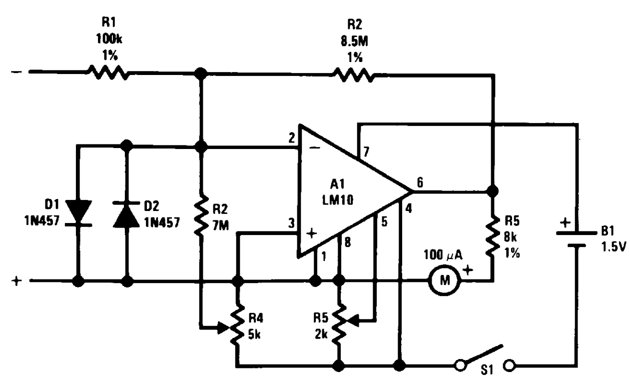
Flashes Above 1.2V
Rate Increases With
Voltage

Figure 66. Single-cell Voltage Monitor



Flash Rate Increases
Above 6V and Below 15V

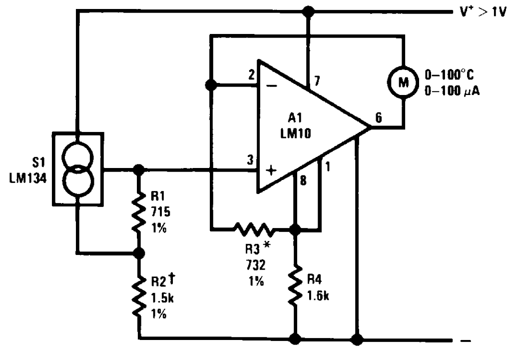
Figure 67. Double-ended Voltage Monitor



INPUT
10 mV, 100nA
FULL-SCALE

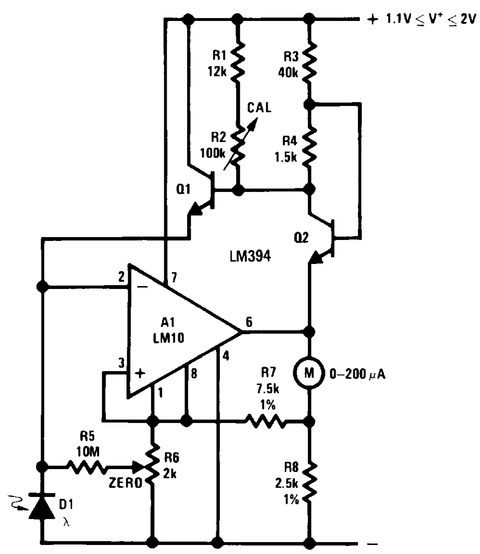
Figure 68. Meter Amplifier

(Pin numbers are for devices in 8-pin packages)



*Trim For Span
†Trim For Zero

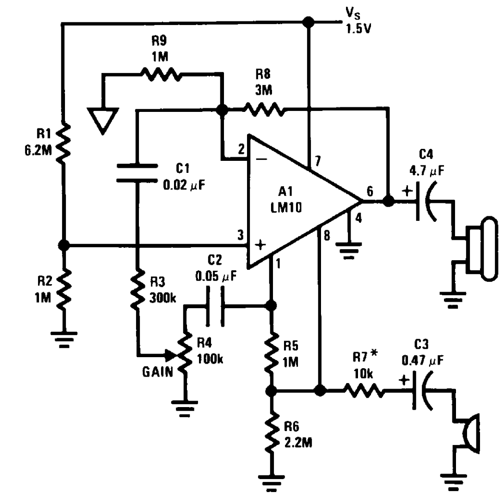
Figure 69. Thermometer



$1 \leq \lambda/\lambda_0 \leq 10^5$

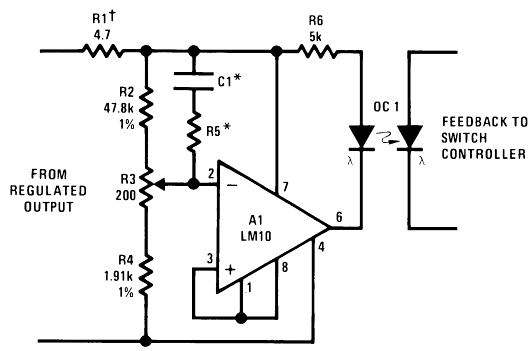
Figure 70. Light Meter

(Pin numbers are for devices in 8-pin packages)



Z_{OUT}~680Ω @ 5 kHz
A_V≤1k
f_1~100 Hz
f_2~5 kHz
R_L~500
*Max Gain Trim

Figure 71. Microphone Amplifier



†Controls “Loop Gain”
*Optional Frequency Shaping

Figure 72. Isolated Voltage Sensor

(Pin numbers are for devices in 8-pin packages)

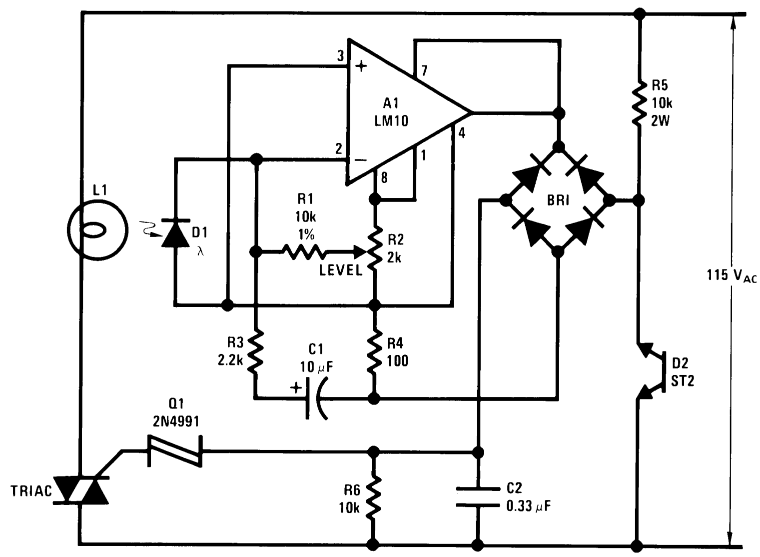


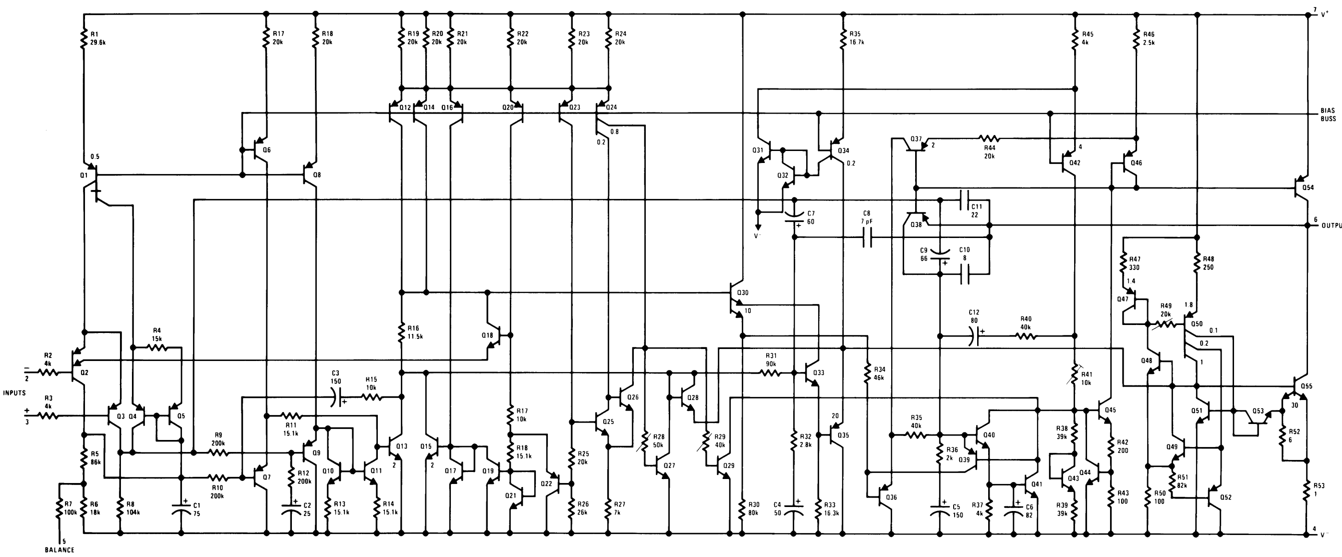
Figure 73. Light-level Controller

APPLICATION HINTS

With heavy amplifier loading to V⁻, resistance drops in the V⁻ lead can adversely affect reference regulation. Lead resistance can approach 1Ω. Therefore, the common to the reference circuitry should be connected as close as possible to the package.

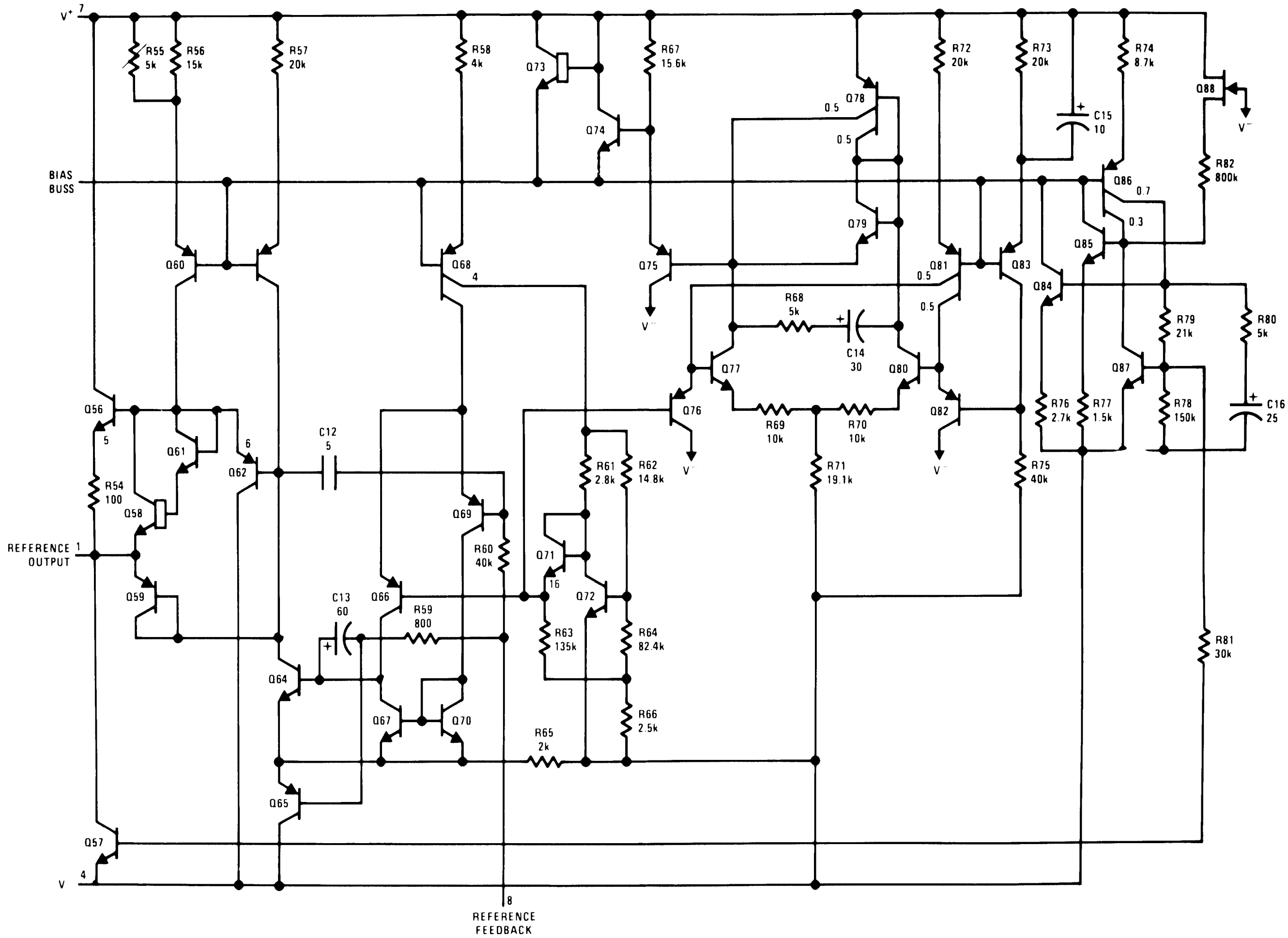
Operational Amplifier Schematic

(Pin numbers are for 8-pin packages)



Reference and Internal Regulator

(Pin numbers are for 8-pin packages)


V+ 7
BIAS BUSS
REFERENCE OUTPUT 1
V- 4
8 REFERENCE FEEDBACK
R55 5k
R56 15k
R57 20k
R58 4k
R67 15.6k
R72 20k
R73 20k
R74 8.7k
R82 800k
R54 100
R59 800
R60 40k
R61 2.8k
R62 14.8k
R63 135k
R64 82.4k
R65 2k
R66 2.5k
R68 5k
R69 10k
R70 10k
R71 19.1k
R75 40k
R76 2.7k
R77 1.5k
R78 150k
R79 21k
R80 5k
R81 30k
C12 5
C13 60
C14 30
C15 10
C16 25
Q56
Q57
Q58
Q59
Q60
Q61
Q62
Q64
Q65
Q66
Q67
Q68
Q69
Q70
Q71
Q72
Q73
Q74
Q75
Q76
Q77
Q78
Q79
Q80
Q81
Q82
Q83
Q84
Q85
Q86
Q87
Q88

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	25

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM10BH	ACTIVE	TO	NEV	8	500	TBD	Call TI	Call TI	-40 to 85	LM10BH	Samples
LM10BH/NOPB	ACTIVE	TO	NEV	8	500	Green (RoHS & no Sb/Br)	POST-PLATE	Level-1-NA-UNLIM	-40 to 85	LM10BH	Samples
LM10CH	ACTIVE	TO	NEV	8	500	TBD	Call TI	Call TI	0 to 70	LM10CH	Samples
LM10CH/NOPB	ACTIVE	TO	NEV	8	500	Green (RoHS & no Sb/Br)	POST-PLATE	Level-1-NA-UNLIM	0 to 70	LM10CH	Samples
LM10CLN	LIFEBUY	PDIP	P	8	40	TBD	Call TI	Call TI	0 to 70	LM10CLN	
LM10CLN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 70	LM10CLN	Samples
LM10CN	LIFEBUY	PDIP	P	8	40	TBD	Call TI	Call TI	0 to 70	LM 10CN	
LM10CN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN | Call TI	Level-1-NA-UNLIM	0 to 70	LM 10CN	Samples
LM10CWM	NRND	SOIC	NPA	14	50	TBD	Call TI	Call TI	0 to 70	LM10CWM	
LM10CWM/NOPB	ACTIVE	SOIC	NPA	14	50	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 70	LM10CWM	Samples
LM10CWMX/NOPB	ACTIVE	SOIC	NPA	14	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 70	LM10CWM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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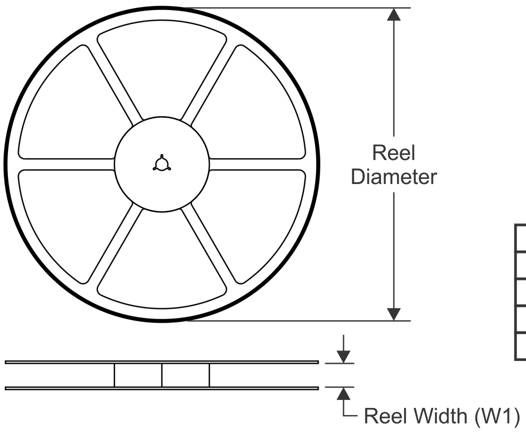
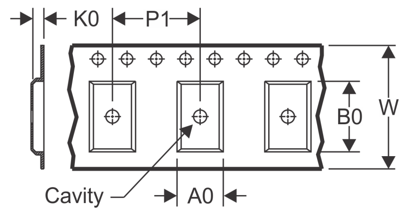
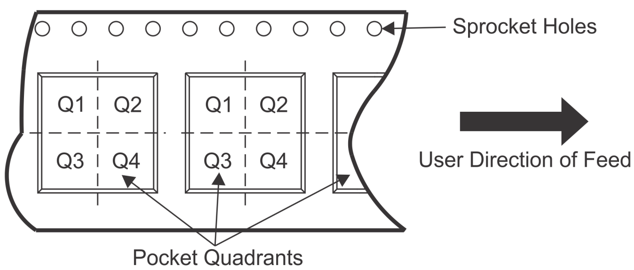
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





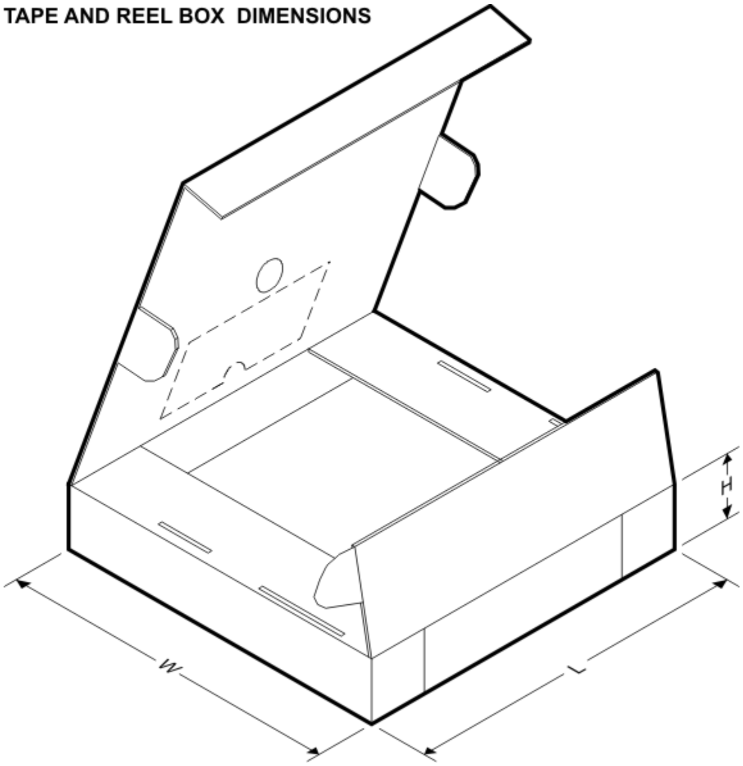
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM10CWMX/NOPB	SOIC	NPA	14	1000	330.0	16.4	10.9	9.5	3.2	12.0	16.0	Q1

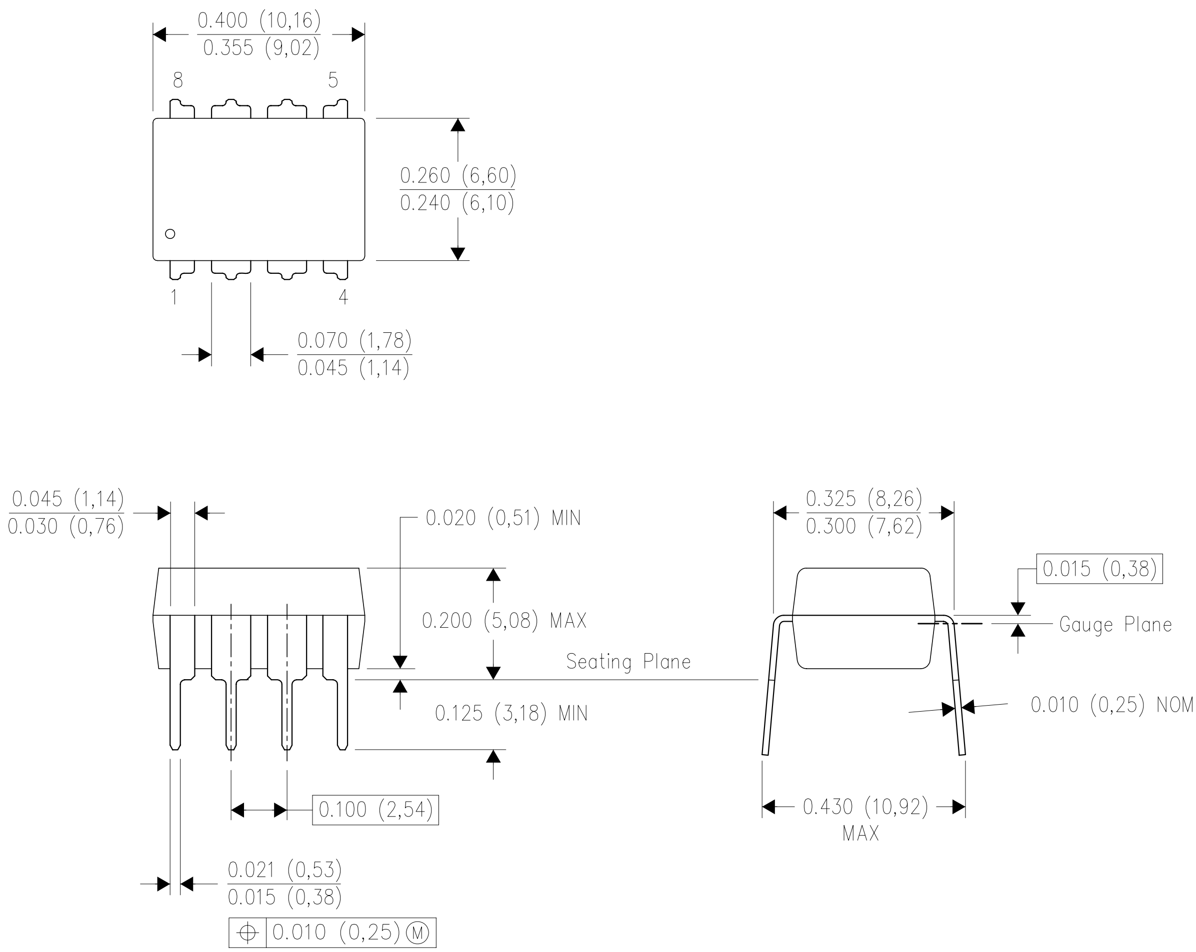
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

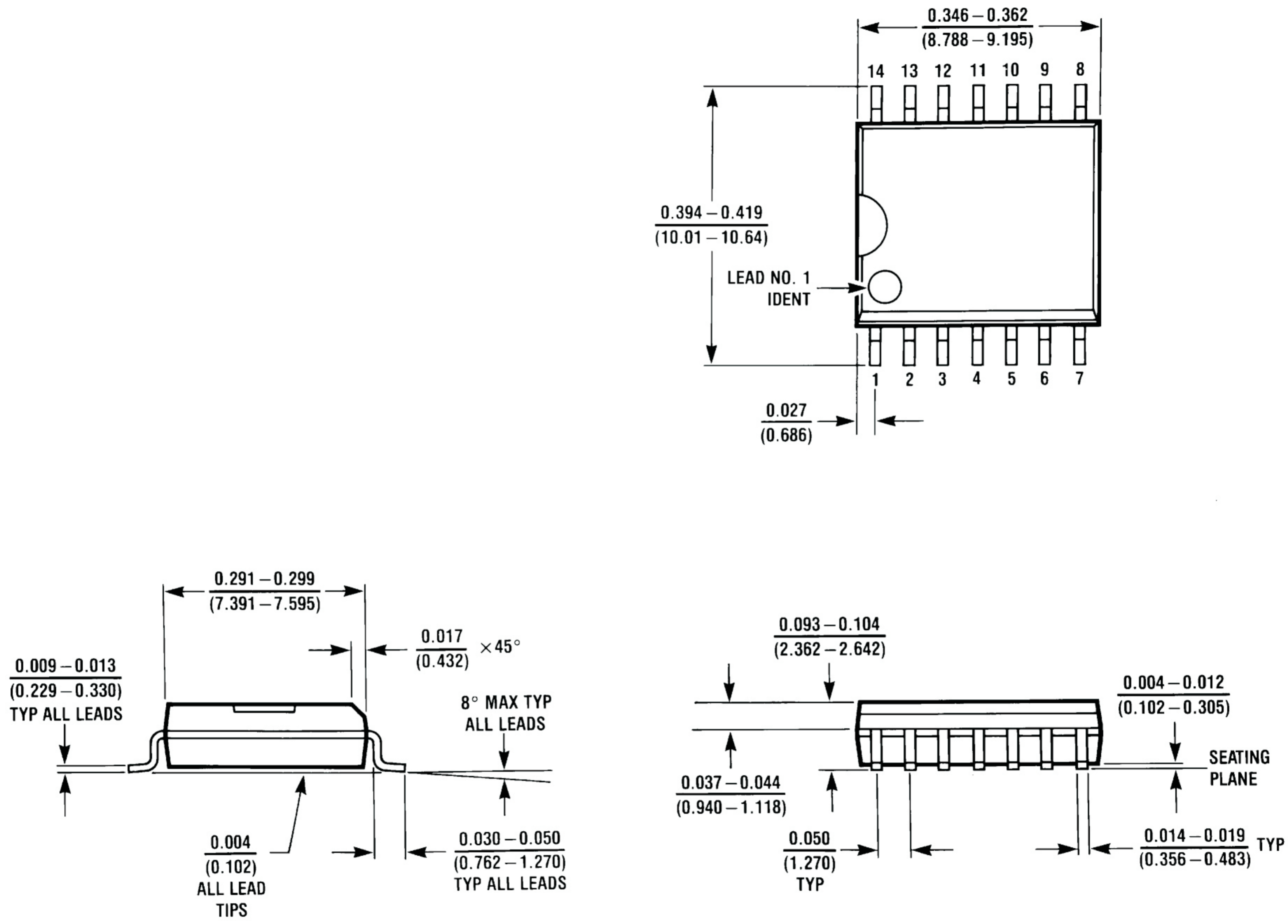
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM10CWMX/NOPB	SOIC	NPA	14	1000	367.0	367.0	38.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



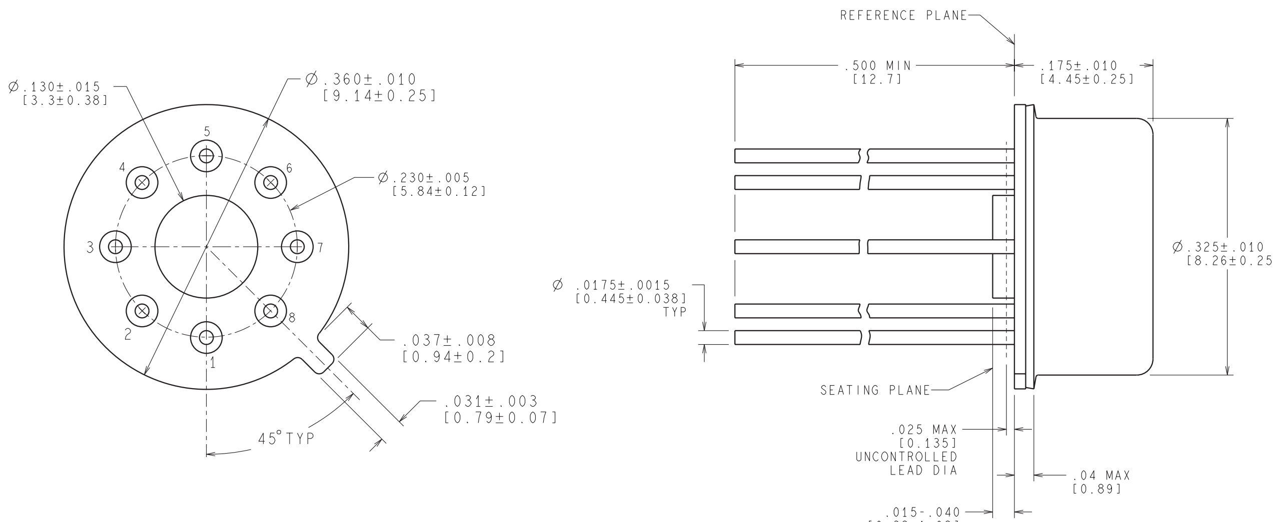
4040082/E 04/2010

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.


0.346 – 0.362
(8.788 – 9.195)
14 13 12 11 10 9 8
0.394 – 0.419
(10.01 – 10.64)
LEAD NO. 1
IDENT
1 2 3 4 5 6 7
0.027
(0.686)
0.291 – 0.299
(7.391 – 7.595)
0.017
(0.432)
× 45°
0.009 – 0.013
(0.229 – 0.330)
TYP ALL LEADS
8° MAX TYP
ALL LEADS
0.004
(0.102)
ALL LEAD
TIPS
0.030 – 0.050
(0.762 – 1.270)
TYP ALL LEADS
0.093 – 0.104
(2.362 – 2.642)
0.004 – 0.012
(0.102 – 0.305)
SEATING
PLANE
0.037 – 0.044
(0.940 – 1.118)
0.050
(1.270)
TYP
0.014 – 0.019
(0.356 – 0.483)
TYP

M14B (REV D)

NEV0008A



MIL-PRF-38535
CONFIGURATION CONTROL

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE IN MILLIMETERS

H08A (REV C)

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